1. Answer the questions below with regard to the state diagram shown.

A) Is this a Mealy or a Moore circuit diagram?

B) What is the output if you start in state 0 and you input the sequence \{0, 1, 1, 1, 0\}?

C) What is the final state if you start in state 0 and input the sequence \{0, 1, 1, 1, 0\}?

D) Show three input sequences with less than 4 terms that will get you from state 3 to state 1.

E) If this state diagram were to be implemented in hardware what is the minimum number of JK flip-flops necessary for the implementation?

2. Draw the Moore state diagram for the following circuit.
3. Fill in the truth table below for the circuit shown. The outputs for X and Y may be either HIGH or LOW, 2 stable states, or they may oscillate.

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>X</th>
<th>Y</th>
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<tbody>
<tr>
<td>0</td>
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</table>

4. In using Verilog explain the difference between a **blocking** and a **non blocking** assignment statement.

5. Draw a sketch using AND, OR, and NOT gates which show the circuit implemented by the following Verilog code.

```verilog
module abc(f,a,b,c);
    input a, b, c;
    output f;
    wire w1;
    and A1(w1, ~a, b);
    or (f, ~w1, ~c);
endmodule
```

6. Write a complete Verilog module which will implement the following circuit.
7. The circuit below has a JK flip-flop and a D flip-flop. If the initial state is 00 find the next two states.
AB = 00. ______________________________

8. Construct a state diagram, state table, K-maps, and draw the circuit diagram of a sequential logic circuit that will operate as follows:

When an input: X = 0 the logic should output the sequence ...00, 01, 10, 11 …repeating
X = 1 the logic should output the sequence …11, 10, 01, 00 …repeating