Mark each of the following as true or false.

1. A sequential circuit must always have inputs in addition to a clock  ____

2. A 4 to 1 multiplexer is a good example of sequential logic.  ____

3. A sequence detector with 30 states requires a minimum of 5 flip flops.  ____

4. In the JK and D sequential circuit below flip flops A, B, and C are in the initial state 0, 1, 0 as shown. List the next four states for the circuit.

   \[
   \begin{array}{ccc}
   J & K & Q \\
   A & B & C \\
   Q & Q & Q \\
   \end{array}
   \]

   \[
   \begin{array}{ccccc}
   \text{State} & A & B & C & Q \\
   \hline
   0 & 0 & 1 & 0 & Q \\
   1 & & & & \\
   2 & & & & \\
   3 & & & & \\
   4 & & & & \\
   \end{array}
   \]

5. Fill in the truth table below for the circuit shown. The output for F may be either HIGH or LOW (2 stable states) or it may oscillate.

   \[
   \begin{array}{ccc}
   A & B & F \\
   \hline
   0 & 1 & \\
   1 & 1 & \\
   1 & 0 & \\
   1 & 1 & \\
   \end{array}
   \]
6. Answer the questions below for the system described by the next state diagram shown.

<table>
<thead>
<tr>
<th>n</th>
<th>n+1</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>B</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

a) Fill in the next state table.

b) Use “D” positive edge triggered flip-flops, fill in the K-maps, and determine the next state equations for the D inputs.

\[
\begin{array}{c|cccc}
\text{D}_A & 00 & 01 & 11 & 10 \\
\text{A} & 0 & 1 & 0 & 1 \\
\end{array} \quad \begin{array}{c|cccc}
\text{D}_B & 00 & 01 & 11 & 10 \\
\text{A} & 0 & 1 & 0 & 1 \\
\end{array} \quad \begin{array}{c|cccc}
\text{Y} & 00 & 01 & 11 & 10 \\
\text{A} & 0 & 1 & 0 & 1 \\
\end{array} \quad \begin{array}{c|cccc}
\text{BX} & 00 & 01 & 11 & 10 \\
\text{A} & 0 & 1 & 0 & 1 \\
\end{array}
\]

\[\text{D}_A = \_\_\_\_\_\] \\
\[\text{D}_B = \_\_\_\_\_\] \\
\[\text{Y} = \_\_\_\_\_\]

7. Given the JK circuit below:

a) Construct the next state table for the circuit below. Take X as the input and A as the output.

\[
\begin{array}{c|cc|c}
\text{Present} & \text{Next} \\
\text{X} & \text{A} & \text{A} \\
\end{array}
\]

\[
\begin{array}{cccc}
\text{X} & \text{A} & \text{A} \\
0 & 0 & 1 & 0 \\
0 & 1 & 1 & 1 \\
1 & 0 & 0 & 0 \\
1 & 1 & 1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|c}
\text{X} & \text{A} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|c}
\text{X} & \text{A} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|c}
\text{X} & \text{A} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|c}
\text{X} & \text{A} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]

\[
\begin{array}{c|c}
\text{X} & \text{A} \\
0 & 0 \\
0 & 1 \\
1 & 0 \\
1 & 1 \\
\end{array}
\]
b) Write the Verilog code that will implement the circuit above:

```verilog
module jk(x, clk, j, k, A);
```

8. Given the Verilog module to the right with the input signals to the module as shown below:

```verilog
module verilogcircuit(clk, D, Q);
output Q;
input clk, D;
reg Q;

always @ (negedge clk)
begin
  Q <= ~D;
end
endmodule
```

Complete the waveform for Q as indicated below.

9. Construct a state diagram, state table, K-maps, and draw the circuit diagram of a sequential logic circuit that will operate as follows:

When an input:  
- X = 0 the logic should output the sequence ...00, 01, 10, 11 ...repeating
- X = 1 the logic should output the sequence ...11, 10, 01, 00 ...repeating