EE 254           Final Exam Review

1. The final exam is open book and open notes. It will be made up of problems similar to those on the previous 3 hour exams. For review, be sure that you can work all of the problems on the old exams.

2. The first section of the final will be short answer. There may be questions from any topic covered in the class. Typical short answer questions are shown below.
   a) Convert $36_{10}$ to base 16.
   b) Explain the difference between sequential logic and combinational logic.
   c) A counter has 10 flip flops. What is the maximum number of states. What is the minimum number of states.
   d) Distinguish between volatile and nonvolatile. In general is dynamic RAM volatile or not.
   e) What is it that determines the number of different instructions that a computer is capable of doing.
   f) How many memory chips are needed to construct a 1 Meg x 32 bit memory system if the chips are 4K x 4.
   g) What are the advantages of microprogramming over hardwired logic.
   h) What is pipelining.

3. The second section of the final will consist of logic problems which you must solve. Most of this section concentrates on analysis rather than design. Typical questions include the following.
   a) Fill in the K-Map and truth table for the function
      \[ f = (AB \cdot D) \cdot (\overline{C} + \overline{A} \cdot \overline{B}) + AC \]

   \[
   \begin{array}{c|c|c|c|c}
   & CD & \hline
   f & 00 & 01 & 11 & 10 \\
   \hline
   00 & & & & \\
   01 & & & & \\
   11 & & & & \\
   10 & & & & \\
   \end{array}
   
   b) Using only algebra, prove or disprove the following:
   \[ B \overline{C} + B C \overline{D} = B \overline{C} \overline{D} + B \overline{D} \]

   c) Fill in the truth table below for the circuit shown. The outputs for X and Y may be either HIGH or LOW, 2 stable states, or they may oscillate.
4. Show how to connect the following PAL such that it implements the function given by:

\[ F = A \cdot B \cdot \overline{C} + B \cdot \overline{C} \cdot D + \overline{A} \cdot \overline{B} \cdot C \cdot \overline{D} + A \cdot \overline{B} \cdot C \cdot D \]

5. In the third section of the final you will be asked to do some design. Typical questions include the following.
   a) Design a 3 bit counter to count in the following sequence
   \[ 000 \rightarrow 001 \rightarrow 100 \rightarrow 101 \rightarrow 110 \rightarrow 000. \]
   b) A combinational logic design problem.

6. A stepping motor requires a two phase digital input as shown in the waveforms below. Design a sequential circuit which will accept a single clock as an input and will produce the two phase signal shown.

7. Design a combinational logic circuit which will produce an output of 1 if and only if the product of two 2-bit numbers is divisible by 3.

8. There will be one problem about microprogramming.

9. Write a complete Verilog module which will implement the following circuit.
10. What circuit does the following Verilog code implement.

```verilog
module Mystery(clk, state, clr);
    parameter n = 4;
    input clk, clr;
    output [n-1:0] state;
    reg [n-1:0] state;
    always@(posedge clk)
        if(clr)
            state <= 0;
        else
            state <= state + 1;
endmodule
```

11. Design a Moore machine which will recognize the sequence 1010.

12. Design a circuit using JK flip flops for the following state diagram.

![State Diagram](image-url)
13. For the circuit below take $Q_A$ and $Q_B$ as the circuit's outputs. Draw the state diagram as a Moore machine.

14. Design a Mealy machine which will output a 1 when it receives either two ones or two zeros on successive clock periods.
1. Which instructions in the following sequence have data dependencies?
   I1: div r1, r2, r3
   I2: sub r4, r1, r5
   I3: ash r2, r6, r7 ; Arithmetic shift
   I4: mul r8, r4, r2
   I5: beq r9, #0, r10 ; Branch if equal
   I6: or r3, r11, r1

2. What are four characteristics of a RISC machine?

3. Give three reasons why a five-stage pipelined machine is not five times faster than the same machine with no pipeline.

4. Answer the questions below about the diagram.
   A) Where does the line marked "select" come from?
   B) What is the purpose of the instruction decoder?
   C) If the op code is 8-bits wide and the average assembly language instruction takes 3 micro-instructions, what is the maximum size of the Micro-code ROM? Assume a 20-bit control word.

5. What are the advantages of microprogramming?
6. Consider the following assembly language instruction sequence that is running on a machine with a 3-stage pipeline. If the JNZ instruction does the jump, which instructions will be flushed from the pipeline?

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LD R1, R3</td>
<td>Load R1 with memory 248</td>
</tr>
<tr>
<td>ADI R1, R1, 3</td>
<td>Add 3 to R1</td>
</tr>
<tr>
<td>NOT R1, R1</td>
<td>Complement R1</td>
</tr>
<tr>
<td>INC R1, R1</td>
<td>Increment R1</td>
</tr>
<tr>
<td>JNZ Target</td>
<td>Jump Not Zero</td>
</tr>
<tr>
<td>INC R3, R3</td>
<td>Increment R3 (address)</td>
</tr>
<tr>
<td>LD R2, R3</td>
<td>Load R2 from memory 249</td>
</tr>
<tr>
<td>ADD R2, R2, R1</td>
<td>Add R1 to R2</td>
</tr>
<tr>
<td>INC R3, R3</td>
<td>Increment R3</td>
</tr>
<tr>
<td>ST R3, R2</td>
<td>Store R2 in memory 250</td>
</tr>
</tbody>
</table>

7. What is indexed addressing?

8. Why do most computers implement register indirect addressing but few implement memory indirect addressing?

9. A machine has 16 bit instructions in the following format.

<table>
<thead>
<tr>
<th>7</th>
<th>3</th>
<th>3</th>
<th>3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Opcode</td>
<td>SR1</td>
<td>DR1</td>
<td>SR2</td>
</tr>
</tbody>
</table>

A) How many different instructions are possible?

B) How many registers does this machine have?