

## Definitions for Programmable Logic Devices

- AHDL - Altera Hardware Description Language. Text-based, high-level design-entry language developed by Altera for its design compilers.
- AND-array - A two-dimensional array of logical signal inputs which are combined at their crosspoints through AND circuits. Each crosspoint therefore provides a two-input AND function.
- Cell - The basic programmable functional element in a PLD architecture, the same as "block".
- CPLD - Complex PLD. A common term for a PLD composed of many blocks where the architecture of the blocks is very much like PALs.
- EEPLD - A PLD that uses EEPROM memory cells to hold the programmable logic configuration (but is of a much higher complexity than the Simple PLD devices).
- EEPROM - E<sup>2</sup>PROM [e-squared]. Electrically Erasable Programmable Read-Only Memory.
- EPLD - A PLD that uses EPROM memory cells rather than fuses, antifuses or RAM- controlled pass transistors to hold the programmed logic configuration. EPLDs may be small or large in functional capacity, but some confusion has equated them improperly with CPLDs because EPLD was the first term popularized for CPLDs.
- EPROM - Erasable Programmable Read-Only Memory.
- Field-programmable - This indicates a device can be programmed in the laboratory of the system engineer rather than at the factory of the integrated circuit manufacturer. PLDs are field programmable, whereas gate arrays are factory programmable.
- Flash - A non-volatile memory silicon technology used in many PLD and CPLD devices. The technology allows higher reliability and lower cost devices. The devices are electrically reprogrammable and erasable.
- FPGA - Field Programmable Gate Array. A PLD containing logic elements or cells that are interconnected through signal channels by programmable switches. The cells may vary in complexity from a single gate in some architectures to programmable functions that are the size of larger PAL devices. This type of architecture produces statistically varying results in performance and functional capacity because of the many choices to choose cells and route interconnects, much like gate arrays. The programming means in an FPGA may be reprogrammable (such as SRAMs) or OTP (such as anti-fuses and fuses).
- FPLA - Field Programmable Logic Array. A PLD with both programmable AND and programmable OR terms, but in the complexity range of the Simple PLDs.
- Fuse - A low-resistance circuit element which may be programmed to become an open circuit. The programming is called "blowing" the fuse and is normally done thermally, by surges of relatively high currents.
- HDL - Hardware Description Language. A language for describing logic circuits generally.
- I/O Cell - Logic cells which receive input signals from the device pins or provide output signals to device pins or provide both functions.
- I/OB - Input/Output Block. A logic block in programmable logic that can be configured to be either an input or output or bidirectional I/O pin and can be programmed to provide a number of logic functions and register options.
- ISP - In-System Programmable term pioneered by Lattice Semiconductor refers to programming and reprogramming devices directly on a printed circuit board from a PC, microprocessor, or by ATE. The term "isp" is a common prefix for Lattice product names and numbers.
- JTAG - Joint Test Action Group. An industry standard serial interface used as a test and programming interface in ISP-PLDs.
- LUT - Look Up Table.
- Macrocell - a. A group of logic cells that perform a specified function which is defined in a library of functions in the design system. A macrocell may be "hard" because its configuration is fixed wherever it is placed in the device. Or, it may be "soft" because its topology varies depending on where its placed in the device. b. Fundamental logic block of SPLD or CPLD, may be at an output or buried.
- Mask-programmable - Devices, usually gate arrays, which are programmed at the factory by depositing metal interconnects among the logic elements.
- MPGA - Masked Programmable Gate Array.
- MUX - Multiplexer. A digital circuit that selects one or more inputs from a larger number of inputs.
- NETLIST - A shorthand description for a schematic indicating connections among logic elements, usually expressed in EDIF format.

NOR-array - A two-dimensional array of logical signal inputs which are combined at their crosspoints through NOR circuits. Each crosspoint therefore provides a two-input NOR function.

OR-array - A two-dimensional array of logical signal inputs which are combined at their crosspoints through OR circuits. Each crosspoint therefore provides a two-input OR function.

OTP - One-time Programmable. A term referring to fuse-based devices that cannot be erased and, therefore, can be used only once.

Output Macrocell - A Macrocell function which provides a signal at an output pin.

PAL - Programmable Array Logic. A PLD architecture that simplified PLAs by fixing the OR array and maintaining the programmable AND array. An AMD trademark but originated by Monolithic Memories Inc.

PEEL - Programmable Electrically Erasable Logic. ICT family of EEPLD devices.

PLA - Programmable Logic Array. An architecture using a programmable AND array in series with a programmable OR array.

PLC - Programmable Logic Cell is the major logic building block for the ORCA FPGA architecture from Lucent Technologies (formerly AT&T). Each PLC contains a PFU and routing resources for logic implementation.

PLD - A logic device that can be configured by a system designer in the laboratory with readily available means. This is a general term although it is often used to indicate only small PLDs such as PALs and FPLAs.

PLD Assemblers - An early type of design tool that can convert sum-of-products design equations into fuse-programming data.

PLD Compilers - Design tools that support a variety of design-entry techniques and sometimes include logic synthesis capabilities.

Product of Sums - A logic expression describing the output of an array of OR gates followed by an array of AND gates.

Product Term - The output of an AND array.

Programmable - Having the ability to be configured, to be programmed to a desired configuration.

Programmable Element - The switches or fuses which accomplish the interconnection among the logic elements in a PLD.

PROM - Programmable Read-Only Memory. See ROM.

RAM-based - A reprogrammable PLD in which the programming technology is the same as used for volatile memory ICs, usually SRAMs.

Sum of Products - A logic expression describing the output of an array of AND gates followed by an array of OR gates.

TQFP - Thin Quad Flat Pack. A small package used predominantly in PCMCIA applications.

VERILOG - Cadence's high-level hardware description design-entry language.

VHDL - VHSIC Hardware Description Language. An HDL developed under the Department of Defense VHSIC program.