The ARM (Advanced RISC Machine) is a 32-bit microcontroller created by a consortium of companies and manufactured in many different versions. It is widely used in modems, cell phones, personal audio, pagers, cameras, and many more embedded high end applications.

ARM is produced by many different companies and each adds its own variations. We will use the ARM Cortex M0 produced by Philips as the LPC 1114.

RISC – Reduced Instruction Set Computer.

RISC/CISC controversy and history
- In the 1970s as IC manufacturers were able to put more and more on a single chip, computer architects needed to decide what to do with the extra space.
- The prevailing idea was to create more complex instructions which are then executed in microcode. This reduces the use of program memory to fetch instructions and should run faster. This was called CISC for Complex Instruction Set Computer.
- A counter idea, created by IBM, was to use the extra space for things like more registers, cache memory, and numerical processing ability. This solution kept the instruction set very simple so that it took up little extra circuitry. This was called RISC and began about 1980.
- Many new RISC machines were built such as the SUN Sparc. The Intel x86 line represents an architecture that leans toward the CISC side.
- By the mid-1990s it was clear that the ideal machine was neither RISC nor CISC but something in between. Today most machines have features of both.

Generic RISC features:
- A large number of general purpose registers along with compiler technology to optimize register usage.
- A limited and simple instruction set
- An emphasis on optimizing the instruction pipeline
- Load and store architecture with simple addressing modes

Today, most CPU's have some RISC-like features but pure RISC machines are uncommon. The ARM processor has its origins in 1983 from Acorn Computers Ltd. In 1990 Acorn spun off a new company called Advanced RISC Machines Ltd. which licenses its ARM core to other companies for manufacture. Many other companies now make versions of the ARM processor including Intel, Atmel, Texas Instruments,
FreeScale, and many others. The Cortex M0 is one of the more successful versions of the ARM processor and has recently become available in a 28-pin DIP.

**Feature Summary ARM Cortex M0 core**
- 32-bit RISC processor (32-bit data & address bus)
- Big and Little Endian operating modes
- High performance RISC
- Low power consumption
- Fully static operation
- Fast interrupt response for real-time applications
- Excellent high-level language support
- Simple but powerful instruction set

The instruction set has just 56 instructions in 11 functional groups
- Data move
- Memory access
- Stack operators
- Arithmetic operators
- Logical operators
- Shift and rotate instructions
- Extend instruction and reverse order instructions
- Flow control (branch and calls)
- Memory barrier instructions
- Exceptions related instructions
- Miscellaneous

Note that there is no division instruction in the assembly code – this has to be done piecemeal in software. Likewise, there are no I/O instructions – all I/O is memory mapped.

**Thumb instructions**
The ARM Cortex M0 is a 32-bit computer so one would expect that all of the instructions would be 32-bits long. But a 32-bit instruction is largely wasted on simple operations that make use of the UART, I²C, and bit manipulation so the ARM series of processors also uses *Thumb* instructions. Thumb instructions are 16-bit versions of 32-bit instructions that save considerable program space. A 32-bit ARM *ADD* instruction might look like this: ADD R1, R2, R3. This instruction adds R2 to R3 and puts the result in R1. The thumb version of this instruction is just ADD R1, R2 which add R1 to R2 and puts the result in R3. The result is a slightly less powerful instruction (in some cases) in half of the space. All ARM processors support the Thumb mode.

In some cases, 32-bit instructions are necessary so a third set of instructions called *Thumb2* instructions have been created. Thumb2 instructions are mostly 16-bit instructions with a few 32-bit instructions. The ARM Cortex M0 uses the Thumb2 instruction set. Of the 56 instructions, just 6 are 32-bit. All of the others are 16-bit.
**Data Types**

This processor supports bytes, half-words (16-bits), and full words (32-bits). Bits and nibbles are not supported but can be done with bit manipulation and the logical instructions. All data must begin on a 32-bit word boundary in memory. Instruction fetches are half-word aligned since they are mostly 16-bit.

**ARM Cortex M0 Processor**

**Programmer's Model**

R0-R12 are called general purpose registers. For most of the thumb instruction set only the low registers, R0-R7 are available. The MOV instructions have access to all of the registers.

Register R13 is the stack pointer. The lower two bits of this register is always zero since it accesses the stack on 32-bit word boundaries.
Register R14 is called the link register. For quick access to subroutines the link register is effectively a 1 level stack. The return address of a call instruction is saved in this register. If a subroutine itself makes another call its return address then goes on the stack. One level subroutine calls are thus much faster.

Register R15 is the program counter. It is 32-bits long and there is a linear address space from 0 to $2^{32}-1$.

The CPU flags are stored in the program status register APSR.

**Memory mapping**

![Memory Map for Cortex M0 Processor](image-url)
**Code Region (0x00000000—0xFFFFFFFF)**

The size of the code region is 512 MB. It is primarily used to store program code, including the exception vector table, which is a part of the program image. It can also be used for data memory (connection to RAM).

**SRAM Region (0x20000000—0x3FFFFFFF)**

The SRAM region is located in the next 512 MB of the memory map. It is primarily used to store data, including stack. It can also be used to store program code. For example, in some cases you might want to copy program code from slow external memory to the SRAM and execute it from there. Despite the name given to this region (it is called “SRAM”), the actual memory devices being used could be SRAM, SDRAM, or some other type.

**Peripheral Region (0x40000000—0x5FFFFFFF)**

The peripheral region also has the size of 512 MB. It is primarily used for peripherals and can also be used for data storage. However, program execution is not allowed in the peripheral region. The peripherals connected to this memory region can be either the AHB-Lite peripheral or APB peripherals (via a bus bridge).

**RAM Region (0x60000000—0x9FFFFFFF)**

The RAM region consists of two 512 MB blocks, which results in total of 1 GB of space. Both 512 MB memory blocks are primarily used to stored data, and in most cases the RAM region can be used as a 1 GB continuous memory space. The RAM region can also be used for program code execution. The only differences between the two halves of the RAM region is the memory attributes, which might cause differences in cache behavior if a system-level cache (level-2 cache) is used. Memory attributes will be covered in more detail later in this chapter.

**Device Region (0xA0000000—0xDFFFFFFF)**

The external device region consists of two 512 MB memory blocks, which results in a total of 1 GB of space. Both 512 MB memory blocks are primarily used for peripherals and I/O usage. The device region does not allow program execution, but it can be used for general data storage. Similarly to the RAM region, the two halves of the device region have different memory attributes.

**Internal Private Peripheral Bus (PPB) (0xE0000000—0xE000FFFF)**

The internal PPB memory space is allocated for peripherals inside the processor, such as the interrupt controller NVIC, as well as the debug components. The internal PPB memory space is 1 MB in size, and program execution is not allowed in this memory range.

Within the PPB memory range, a special range of memory is defined as the System Control Space (SCS). The SCS address is from 0xE000E000 to 0xE000FFFF. It contains the interrupt control registers, system control registers, debug control registers, and the like. The NVIC registers are part of the SCS memory space. The SCS also contains an optional timer called the SysTick. This will be covered in Chapter 10.

**Reserved Memory Space (0xE1000000—0xFFFFFFFF)**

The last section of the memory map is a 511 MB reserved memory space. This may be reserved in some microcontrollers for vendor-specific usages.
LPC1114 from NXP
FEATURES

Processor
ARM Cortex-M0 processor, running at frequencies of up to 50 MHz.

Interrupts
ARM Cortex-M0 built-in Nested Vectored Interrupt Controller (NVIC).
Non-Maskable Interrupt (NMI).

Memory:
32 kB on-chip flash programming memory.
8 kB SRAM.

Programming
In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software. Flash is programmed with a hex file using Flash Magic.

Digital peripherals:
GPIO pins can be used as edge and level sensitive interrupt sources.
High-current output driver (20 mA) on one pin.
High-current sink drivers (20 mA) on two I²C-bus pins in Fast-mode Plus

Timers
Two 16-bit counter/timers
Two 32-bit counter/timers

Analog peripherals:
10-bit ADC with input multiplexing among 5, 6, or 8 pins depending on package size.

Serial interfaces:
UART with fractional baud rate generation, internal FIFO, and RS-485 support.
SPI controller with SSP features and with FIFO and multi-protocol capabilities
I²C-bus interface supporting full I²C-bus specification and Fast-mode Plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.

Clock generation:
24-bit System tick timer
12 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
Crystal oscillator with an operating range of 1 MHz to 25 MHz.
Programmable watchdog oscillator with a frequency range of 9.4 kHz to 2.3 MHz.
PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the system oscillator or the internal RC oscillator.
Clock output function with divider that can reflect the system oscillator clock, IRC clock, CPU clock, and the Watchdog clock.

Power control:
Integrated PMU (Power Management Unit) to minimize power consumption during Sleep, Deep-sleep, and Deep power-down modes.
Power profiles residing in boot ROM allowing to optimize performance and minimize power consumption for any given application through one simple function call. (LPC1100L and LPC1100XL series only.)
Three reduced power modes: Sleep, Deep-sleep, and Deep power-down.
Processor wake-up from Deep-sleep mode via a dedicated start logic using up to 13 of the functional pins.

Power-On Reset (POR).

Brownout detect with up to four separate thresholds for interrupt and forced reset.

Unique device serial number for identification.

Single power supply (1.8 V to 3.6 V).

DIP 28 pin package.

28-pin DIP package for LPC1114