

The program below uses Timer 3 and operates on an output bit. Use the register information on the succeeding pages to answer the questions below. Assume the ARM Discovery board is running at 16 MHz.

1. Which output bit is being operated on and how is it changing?

2. What is the purpose of the variable `tmp`?

3. What does line 8 do? `TIM3_CR1 |= (1 << 7);`

4. What does line 9 do? `TIM3_CR1 |= (1 << 3);`

5. What does line 10 do? `TIM3_PSC = 0;`

6. What does line 11 do? `TIM3_ARR = 16000;`

7. What does line 12 do? `TIM3_CR1 |= 1;`

8. What do lines 17 and 18 do?

```
while((TIM3_CR1 & 1) != 0);  
TIM3_CR1 |= 1;
```

9. What is the frequency of the output signal?

```
1 #include "stm32f407vg.h"
2 int main()
3 {int tmp;
4   RCC_AHB1ENR |= 1;
5   RCC_APB1ENR |= 2;
6   GPIOA_MODER |= 0x0400;
7   GPIOA_OSPEEDER |= 0x0C00;
8   TIM3_CR1 |= (1 << 7);
9   TIM3_CR1 |= (1 << 3);
10  TIM3_PSC = 0;
11  TIM3_ARR = 16000;
12  TIM3_CR1 |= 1;
13  tmp = 0;
14  while(1)
15    {GPIOA_ODR = tmp;
16     tmp = ~tmp;
17     while((TIM3_CR1 & 1) != 0);
18     TIM3_CR1 |= 1;
19    }
20 }
21
```

18.4.1 TIMx control register 1 (TIMx_CR1)

Address offset: 0x00

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Reserved						CKD[1:0]	ARPE	CMS		DIR	OPM	URS	UDIS	CEN	
						r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	r/w	

Bits 15:10 Reserved, must be kept at reset value.

Bits 9:8 **CKD**: Clock division

This bit-field indicates the division ratio between the timer clock (CK_INT) frequency and sampling clock used by the digital filters (ETR, Tlx).

00: $t_{DTS} = t_{CK_INT}$

01: $t_{DTS} = 2 \times t_{CK_INT}$

10: $t_{DTS} = 4 \times t_{CK_INT}$

11: Reserved

Bit 7 **ARPE**: Auto-reload preload enable

0: TIMx_ARR register is not buffered

1: TIMx_ARR register is buffered

Bits 6:5 **CMS**: Center-aligned mode selection

00: Edge-aligned mode. The counter counts up or down depending on the direction bit (DIR).

01: Center-aligned mode 1. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set only when the counter is counting down.

10: Center-aligned mode 2. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set only when the counter is counting up.

11: Center-aligned mode 3. The counter counts up and down alternatively. Output compare interrupt flags of channels configured in output (CCxS=00 in TIMx_CCMRx register) are set both when the counter is counting up or down.

Note: It is not allowed to switch from edge-aligned mode to center-aligned mode as long as the counter is enabled (CEN=1)

Bit 4 **DIR**: Direction

0: Counter used as upcounter

1: Counter used as downcounter

Note: This bit is read only when the timer is configured in Center-aligned mode or Encoder mode.

Bit 3 **OPM**: One-pulse mode

0: Counter is not stopped at update event

1: Counter stops counting at the next update event (clearing the bit CEN)

Bit 2 **URS**: Update request source

This bit is set and cleared by software to select the UEV event sources.

0: Any of the following events generate an update interrupt or DMA request if enabled.

These events can be:

- Counter overflow/underflow
- Setting the UG bit
- Update generation through the slave mode controller

1: Only counter overflow/underflow generates an update interrupt or DMA request if enabled.

Bit 1 **UDIS**: Update disable

This bit is set and cleared by software to enable/disable UEV event generation.

0: UEV enabled. The Update (UEV) event is generated by one of the following events:

- Counter overflow/underflow
- Setting the UG bit
- Update generation through the slave mode controller

Buffered registers are then loaded with their preload values.

1: UEV disabled. The Update event is not generated, shadow registers keep their value (ARR, PSC, CCRx). However the counter and the prescaler are reinitialized if the UG bit is set or if a hardware reset is received from the slave mode controller.

Bit 0 **CEN**: Counter enable

0: Counter disabled

1: Counter enabled

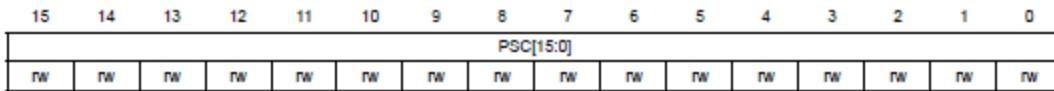
Note: External clock, gated mode and encoder mode can work only if the CEN bit has been previously set by software. However trigger mode can set the CEN bit automatically by hardware.

CEN is cleared automatically in one-pulse mode, when an update event occurs.

18.4.11 TIMx prescaler (TIMx_PSC)

Address offset: 0x28

Reset value: 0x0000



Bits 15:0 **PSC[15:0]**: Prescaler value

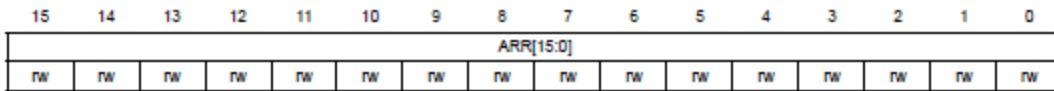
The counter clock frequency CK_CNT is equal to $f_{CK_PSC} / (PSC[15:0] + 1)$.

PSC contains the value to be loaded in the active prescaler register at each update event.

18.4.12 TIMx auto-reload register (TIMx_ARR)

Address offset: 0x2C

Reset value: 0x0000



Bits 15:0 **ARR[15:0]**: Auto-reload value

ARR is the value to be loaded in the actual auto-reload register.

Refer to the [Section 18.3.1: Time-base unit on page 577](#) for more details about ARR update and behavior.

The counter is blocked while the auto-reload value is null.

Timer interrupts

The program below uses Timer 3 and operates on an output bit. The timer triggers an interrupt. Use the register information on the succeeding pages to answer the questions below. Assume the ARM Discovery board is running at 16 MHz.

1. What is the purpose of the `flag` variable?
2. What does line 7 do? `NVICISER0 |= (1 << 29);`
3. What does line 8 do? `TIM3_DIER |= 1;`
4. What does line 9 do? `TIM3_DIER |= (1 << 6);`
5. What is the purpose of the function in lines 26-29?

```
void TIM3_IRQHandler()  
{  
    flag = 0;  
    TIM3_SR &= 0xFFFE;  
}
```

```
1 #include "stm32f407vg.h"
2 int flag;
3 int main()
4     {int tmp;
5       RCC_AHB1ENR |= 1;
6       RCC_APB1ENR |= 2;
7       NVICISER0 |= (1 << 29);
8       TIM3_DIER |= 1;
9       TIM3_DIER |= (1 << 6);
10      GPIOA_MODER |= 0x0400;
11      GPIOA_OSPEEDER |= 0x0C00;
12      TIM3_CR1 |= (1 << 7);
13      TIM3_PSC = 0;
14      TIM3_ARR = 16000;
15      TIM3_CR1 |= 1;
16      //Main program loop
17      tmp = 0;
18      while(1)
19          {GPIOA_ODR = tmp;
20            tmp = ~tmp;
21            flag = 1;
22            while(flag == 1);
23            TIM3_CR1 |= 1;
24          }
25      }
26 void TIM3_IRQHandler()
27     {flag = 0;
28       TIM3_SR &= 0xFFFE;
29     }
```

18.4.5 TIMx status register (TIMx_SR)

Address offset: 0x10

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Reserved				CC4OF	CC3OF	CC2OF	CC1OF	Reserved		TIF	Res	CC4IF	CC3IF	CC2IF	CC1IF	UIF
				rc_wd	rc_wd	rc_wd	rc_wd			rc_wd		rc_wd	rc_wd	rc_wd	rc_wd	rc_wd

Bits 15:13 Reserved, must be kept at reset value.

Bit 12 **CC4OF**: Capture/Compare 4 overcapture flag
refer to CC1OF description

Bit 11 **CC3OF**: Capture/Compare 3 overcapture flag
refer to CC1OF description

Bit 10 **CC2OF**: Capture/compare 2 overcapture flag
refer to CC1OF description

Bit 9 **CC1OF**: Capture/Compare 1 overcapture flag
This flag is set by hardware only when the corresponding channel is configured in input capture mode. It is cleared by software by writing it to '0'.
0: No overcapture has been detected
1: The counter value has been captured in TIMx_CCR1 register while CC1IF flag was already set

Bits 8:7 Reserved, must be kept at reset value.

Bit 6 **TIF**: Trigger interrupt flag
This flag is set by hardware on trigger event (active edge detected on TRGI input when the slave mode controller is enabled in all modes but gated mode. It is set when the counter starts or stops when gated mode is selected. It is cleared by software.
0: No trigger event occurred
1: Trigger interrupt pending

Bit 5 Reserved, must be kept at reset value.

Bit 4 **CC4IF**: Capture/Compare 4 interrupt flag
refer to CC1IF description

Bit 3 **CC3IF**: Capture/Compare 3 interrupt flag
refer to CC1IF description

Bit 2 **CC2IF**: Capture/Compare 2 interrupt flag
refer to CC1IF description

Bit 1 **CC1IF**: Capture/compare 1 interrupt flag

If channel CC1 is configured as output:

This flag is set by hardware when the counter matches the compare value, with some exception in center-aligned mode (refer to the CMS bits in the TIMx_CR1 register description). It is cleared by software.

0: No match

1: The content of the counter TIMx_CNT matches the content of the TIMx_CCR1 register.

When the contents of TIMx_CCR1 are greater than the contents of TIMx_ARR, the CC1IF bit goes high on the counter overflow (in upcounting and up/down-counting modes) or underflow (in downcounting mode)

If channel CC1 is configured as input:

This bit is set by hardware on a capture. It is cleared by software or by reading the TIMx_CCR1 register.

0: No input capture occurred

1: The counter value has been captured in TIMx_CCR1 register (An edge has been detected on IC1 which matches the selected polarity)

Bit 0 **UIF**: Update interrupt flag

* This bit is set by hardware on an update event. It is cleared by software.

0: No update occurred.

1: Update interrupt pending. This bit is set by hardware when the registers are updated:

* At overflow or underflow (for TIM2 to TIM5) and if UDIS=0 in the TIMx_CR1 register.

* When CNT is reinitialized by software using the UG bit in TIMx_EGR register, if URS=0 and UDIS=0 in the TIMx_CR1 register.

When CNT is reinitialized by a trigger event (refer to the synchro control register description), if URS=0 and UDIS=0 in the TIMx_CR1 register.

18.4.4 TIMx DMA/Interrupt enable register (TIMx_DIER)

Address offset: 0x0C

Reset value: 0x0000

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	TDE	Res	CC4DE	CC3DE	CC2DE	CC1DE	UDE	Res.	TIE	Res	CC4IE	CC3IE	CC2IE	CC1IE	UIE
	RW		RW	RW	RW	RW	RW		RW		RW	RW	RW	RW	RW

Bit 15 Reserved, must be kept at reset value.

Bit 14 **TDE**: Trigger DMA request enable
 0: Trigger DMA request disabled.
 1: Trigger DMA request enabled.

Bit 13 Reserved, always read as 0

Bit 12 **CC4DE**: Capture/Compare 4 DMA request enable
 0: CC4 DMA request disabled.
 1: CC4 DMA request enabled.

Bit 11 **CC3DE**: Capture/Compare 3 DMA request enable
 0: CC3 DMA request disabled.
 1: CC3 DMA request enabled.

Bit 10 **CC2DE**: Capture/Compare 2 DMA request enable
 0: CC2 DMA request disabled.
 1: CC2 DMA request enabled.

Bit 9 **CC1DE**: Capture/Compare 1 DMA request enable
 0: CC1 DMA request disabled.
 1: CC1 DMA request enabled.

Bit 8 **UDE**: Update DMA request enable
 0: Update DMA request disabled.
 1: Update DMA request enabled.

Bit 7 Reserved, must be kept at reset value.

Bit 6 **TIE**: Trigger interrupt enable
 0: Trigger interrupt disabled.
 1: Trigger interrupt enabled.

Bit 5 Reserved, must be kept at reset value.

Bit 4 **CC4IE**: Capture/Compare 4 interrupt enable
 0: CC4 interrupt disabled.
 1: CC4 interrupt enabled.

Bit 3 **CC3IE**: Capture/Compare 3 interrupt enable
 0: CC3 interrupt disabled
 1: CC3 interrupt enabled

Bit 2 **CC2IE**: Capture/Compare 2 interrupt enable
 0: CC2 interrupt disabled
 1: CC2 interrupt enabled

Bit 1 **CC1IE**: Capture/Compare 1 interrupt enable
 0: CC1 interrupt disabled
 1: CC1 interrupt enabled

Bit 0 **UIE**: Update interrupt enable
 0: Update interrupt disabled
 1: Update interrupt enabled