Revised: December 15, 2018

CS 320 **Spring 2018/19**
Computer Architecture **Dr. Blandford**

Text: Computer Organization and Architecture 10th edition, by William Stallings, Prentice-Hall, 2016.

References:

1. Computer Architecture by Robert J. Baron and Lee Higbie, Addison-Wesley, 1992.

Grading: There will be 3 hour long exams, homework assignments, and a 2 hour comprehensive final exam. The hour exams will count 20% each, the homework assignments will count 10%, the final will count 20%. In class participation in discussion will be graded and will count 10%.

Class Participation: Each student will be responsible for the days reading assignment and class participation.

The final exam will be given on Monday, May 6 at 11:00am

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CS 320 **Dr. Blandford**

Computer Architecture **Spring 2018/19**

Monday	Wednesday	Friday
Jan. 14 Ch1 pp. 2-42 Introduction and overview http://williamstallings.com/StudentSupport.html	**Jan. 16 Ch 2 pp 46-74** x-86, embedded systems ARM	**Jan. 18 Ch 1-2** Discussion
Jan. 21 **Martin Luther King Day**	**Jan. 23 Ch 3 pp 81-116** Computer function, interrupts, memory, busses, arbitration	**Jan. 25 Ch4 pp120-152** Cache memory systems
Jan. 28 Ch4 pp 121-152 Cache memory, replacement algorithms. Pentium 4 cache	**Jan. 30 Ch 3-4** Discussion	**Feb. 1 Ch 1-4** **Hour Exam 1**
Feb. 4 Review exam	**Feb. 6 Ch 5 pp 166-190** Memory hardware and organization, rambus, cache ram	**Feb. 8 Ch 6 pp 194-224** Flash memory, solid state drives, Magnetic disks, RAID
Feb. 11 Ch 5, 6 Discussion	**Feb. 13 Ch7 pp229-270** Programmed I/O, interrupts, I/O channels, DMA, Direct Cache access	**Feb. 15 Ch 7** Discussion
Feb. 18 Ch 8 pp 276-298 Operating systems, multi-programming, scheduling X86 memory management	**Feb. 20 Ch 5-8** Discussion	**Feb. 22 Ch 5-8** **Hour Exam 2**
Feb. 25 Review exam	**Feb. 27 Ch 10 pp 329-367** Arithmetic, integer multiply and divide, floating point	**Mar. 1 Ch 10** Discussion
Mar. 4 Ch 12 pp412-438 Instructions and operations X86 and ARM data types	**Ch 12/13 pp438-484** X86 and ARM instruction set Types of operations Addressing modes	**Mar. 8 Ch 12, 13** Discussion
Mar. 11 **Spring Break**	**Mar. 13** **Spring Break**	**Mar. 15** **Spring Break**
Mar. 18 Ch 14 pp489-530 CPU structure, pipelining Register organization	**Mar. 20 Ch 14** Discussion	**Mar. 22 Ch15 536-571** RISC/CISC controversy RISC machines
Mar. 25 Ch15 Discussion	**Mar. 27 Ch16 pp576-607** Intel Core machines ARM Cortex M3/4	**Mar. 29** Discussion
Apr. 1 Ch 10 + 12-16 **Hour Exam**	**Apr. 3** Review exam	**Apr. 5 Ch 20 pp 708-727** Microprogramming Hardwired connections
Apr. 8 Ch 20 pp 708-727 Microprogramming Hardwired connections	**Apr. 10 Ch 21 pp 730-766** Processor control Micro-operations Instruction cycle, CPU controller Intel 8080	**Apr. 12 Ch 20-21** Discussion **Last day to withdraw with a w**
Apr. 15 Ch 17/18 Clusters, Multiple processors Multithreading Parallel processing	**Apr. 17 Ch 18** Multicore processors Core I7- ARM A15	**Apr. 19** **Easter Break**
Apr. 22 Ch 17/18 Discussion	**Apr. 24 Ch 19** GPU operations Graphics processors	**Apr. 26 Ch 19 + Notes** Graphics processors
Apr. 29 Discussion	**May 1** Review	

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CS 320 Syllabus Supplement

Catalog Description Studies the architecture of computer systems from four-bit machines to supercomputers. Memory systems, I/O processors, and multi-computer systems are studied in detail. RISC, CISC and Neural Nets are introduced. Establishes the relationship of hardware and software. Includes hands-on projects. Spring

Credit Hour Policy This course meets the federal requirements of 15 in-class hours plus an expected 30 hours of out-of-class work per credit hour over a semester. (At least 135 hours total; 9 per week)

Time & Place CS 320 meets Monday, Wednesday, and Friday at 11:00 AM in Koch Center 267

Learning Objectives

The objective of this course is to teach students the logical structure of a modern computer system including the control unit, internal and external memory, and I/O.

Course outcomes by program outcome

1b. Students will understand the fundamentals of their major field of study.

- All students will participate in discussions of the following topics:
  Von Neuman architecture
  memory systems
  bus structures
  interrupt and I/O systems
  microprogramming
  RISC and CISC machine architecture
  CPU structure
  ARM Cortex and Pentium architectures
  VLIW Architecture

2c. Students will be able to communicate effectively both orally and in writing.

- Students will write complete explanations of computer architecture concepts in a clear and effective manner.
- Students will complete a formal term paper on a computer architecture topic.
- All students will demonstrate an ability to orally explain topics in computer architecture in a clear and effective manner.

3b. Graduates will be cognizant of contemporary issues.

- Students will be introduced to contemporary professional issues.
- Students will complete a term paper on a contemporary professional issue related to computer architecture.

Homework Problems will be assigned daily. Assignments are posted on the website.

Attendance Policy You are expected to attend all class sessions. Absences may adversely affect your grade.

Office Hours Dr. Blandford's office is Koch Center 266, Campus phone is 2201. He will usually be in his office from 7:00 to 8:00 AM and 2:00-3:00 PM on MWF and from 7:00 to 10:00AM on TT.

Disability Policy It is the policy and practice of the University of Evansville to make reasonable accommodations for students with properly documented disabilities. Students should contact the Office of Counseling and Health Education at 488-2663 to seek services or accommodations for disabilities. Written notification to faculty from the Office of Counseling and Health Education is required for academic accommodations.

Honor code This course will be governed by the University of Evansville Honor Code, which is

I will neither give nor receive unauthorized aid, nor will I tolerate an environment that condones the use of unauthorized aid

This code has two fundamental expectations:

• Students will submit as their own work only those items that are indeed their own work
• Students will hold each other responsible for adhering to the Code