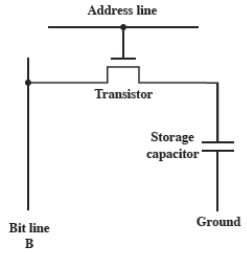
CS 320 **February 2, 2018**
Ch 5 – Memory

Main memory often referred to as core by the older generation because core memory was a mainstay of computers until the advent of cheap semi-conductor memory in the early 1970s.

Random access memory is a term which refers to Read/Write memory. In general it is
Randomly accessed and volatile and read/write.

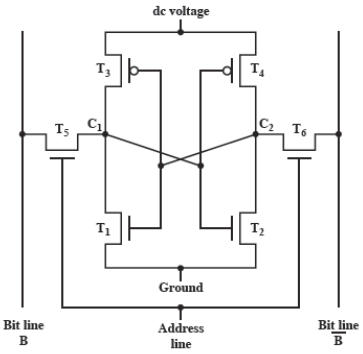
There are two traditional forms of RAM **DRAM and SRAM**

For DRAM **Information stored on capacitors**



(a) Dynamic RAM (DRAM) cell

For SRAM cell can be read or written into information is stored in bistable circuit



(b) Static RAM (SRAM) cell

DRAM cell essentially analog and an SRAM cell essentially digital. **Charged stored on DRAM capacitor can represent any value.**

Characteristics of DRAM to SRAM.
DRAM: volatile, cheap, dense, requires refresh – main memory
SRAM: volatile, faster, requires no refresh – cache

ROM is **Read only memory. It is typically nonvolatile and most often randomly accessed.**

Examples where ROM is used in computer systems include:
Microprogramming, library routines, system programs, function tables

PROM is **Programmable ROM. May be user programmed once. ROM is usually programmed at the factory as part of the fabrication process.**

Read Mostly Memory I **Memory used as ROM but frequently reprogrammed.**

There are three types of PROM.
EPROM, EEPROM, and Flash memory.
EPROM – Erasable PROM. All storage cells erased at once. Can be UV. Somewhat expensive.
EEPROM – Electrically Erasable PROM. Byte or bit erasable but write process is much slower than read.
FLASH – relatively cheap with one transistor per bit. Must erase whole section of memory not just at byte level. Relatively fast erase. Limited (>10,000) erase cycles.

In the figure below
A) This memory is organized as 4M x 4 which means it has **4M words by 4 bits each**
B) The address is multiplexed into rows and columns to save pins.
C) If one address pin is added to the chip e**ach pin handles a row and a col bit so memory goes up by a factor of 4.**
D) RAS and CAS are the **Row address select, Col address select.**
E) The chip size optimized by organization of the memory into a square array of cells because this **reduces decoder size.**
F) Refresh is accomplished as follows: **Disable chip, refresh counter addresses rows, RAS is activated, data is read and written to same address.**
G) The consequences of disabling the chip during refresh means that the c**hip is unavailable about 2% of the time.**

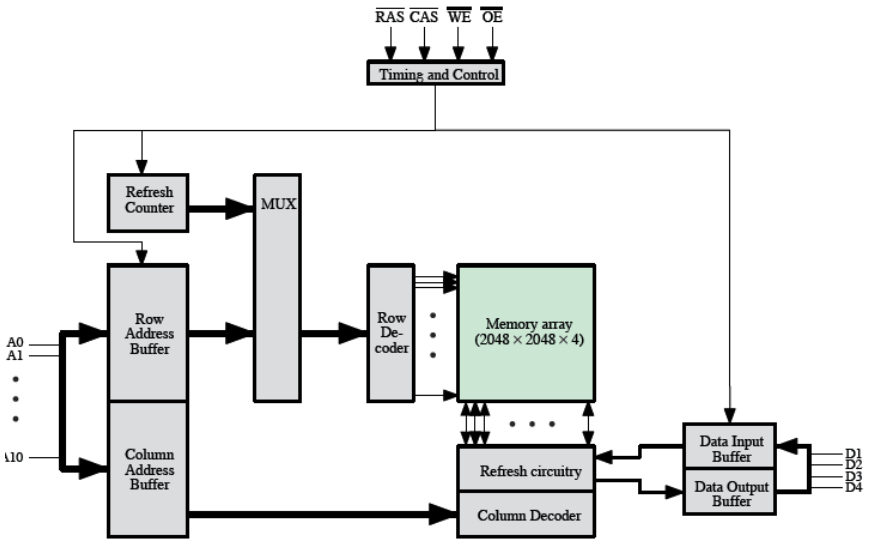


Figure 5.3 Typical 16 Megabit DRAM (4M × 4)

The typical pins you would expect to find on a DRAM chip are: **Address lines, data lines, power ground, RAS, CAS, Write Enable, and Chip or Output Enable.**

The purpose of a Chip Enable pin allows for a **multiple chip systems.**

In the memory system below each chip has 2^{18} bits organized as 512 words with 512 bits per word. The top 9-bits of the address select the word and the bottom 9-bits select the word for output Each chip outputs only one bit. With 8 chips we get a byte out for each 18-bit address. From the outside this memory appears to be 2^{18} x 8

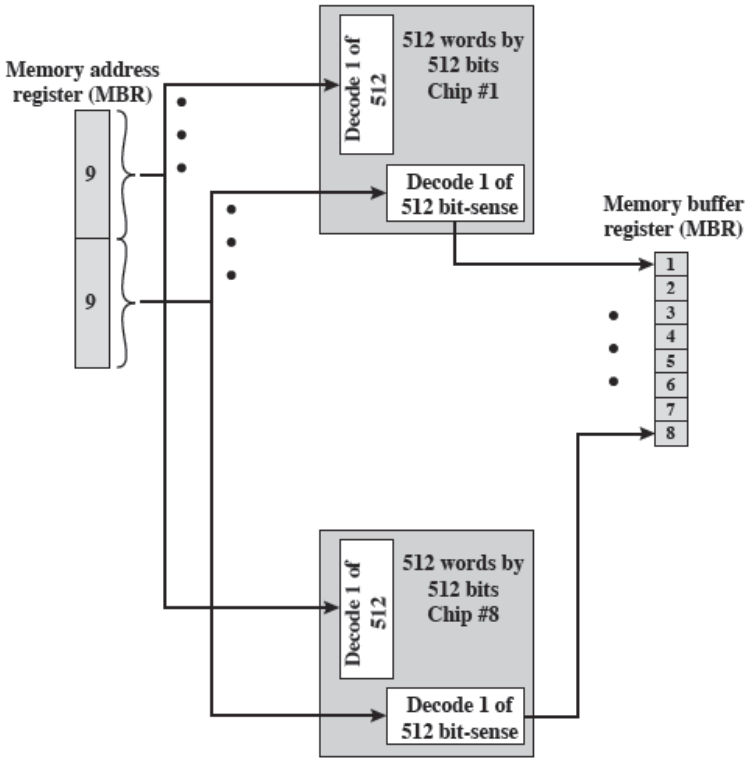


Figure 5.5 256-KByte Memory Organization

In the figure below the memory organization from the outside is 1 M x 8.
There are 8 rows by 4 columns of chips.

The bottom 2-bits of the 20-bit address selects all 8 chips in one column.

Each of these chips puts out one bit to form an 8-bit word for output

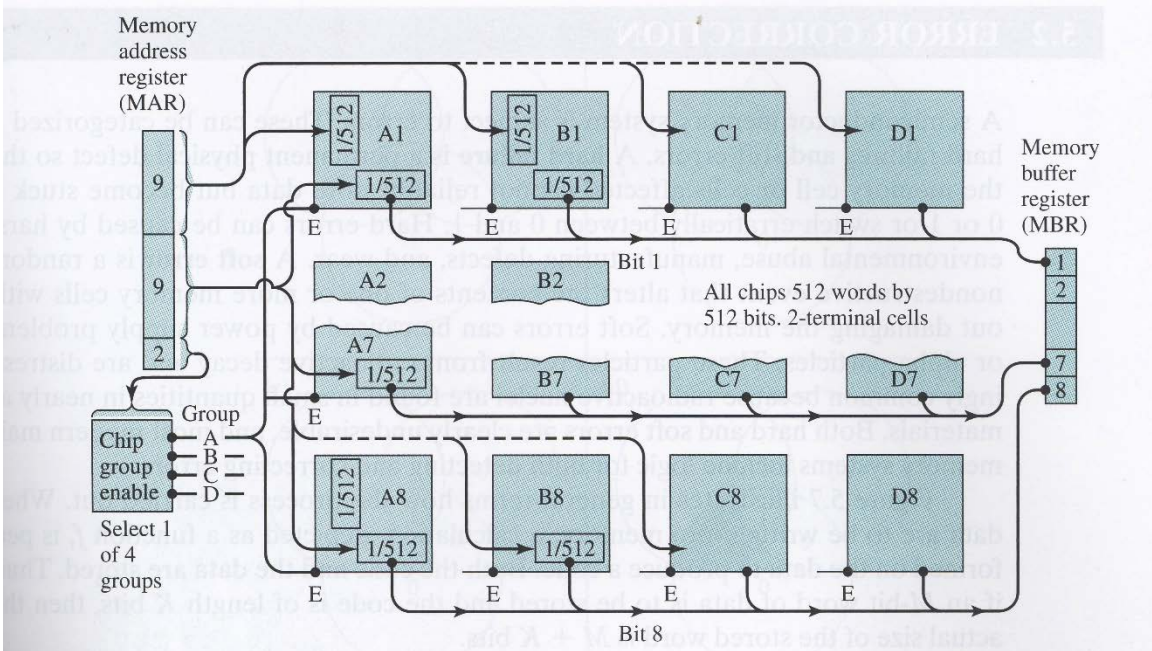


Figure 5.6 1-Mbyte Memory Organization

Error Correction
Memory errors have not seemed like much of a concern to computer architects. Over the last decade or so **Denser memories have made memory errors a more serious problem.**
A memory chip can have a hard failure which is a **Permanent physical failure.**
Or, they can have a soft failure which is a **random nondestructive event that alters a memory cell's contents without damaging it.**

The common sources of soft failures is **Alpha particles and power supply noise.**

A parity bit used to detect an odd number of errors. A parity bit is set to one or zero such that the total number of ones in the number is say even. If any odd number errors occurs the number of ones will be odd. So a parity bit detects an odd number of errors.

The figure below can be used to explain how the Hamming code works. Parity bits are added to each circle A, B, or C to make the total number bits in each circle even. If any bit changes we can detect the error and where it occurred.

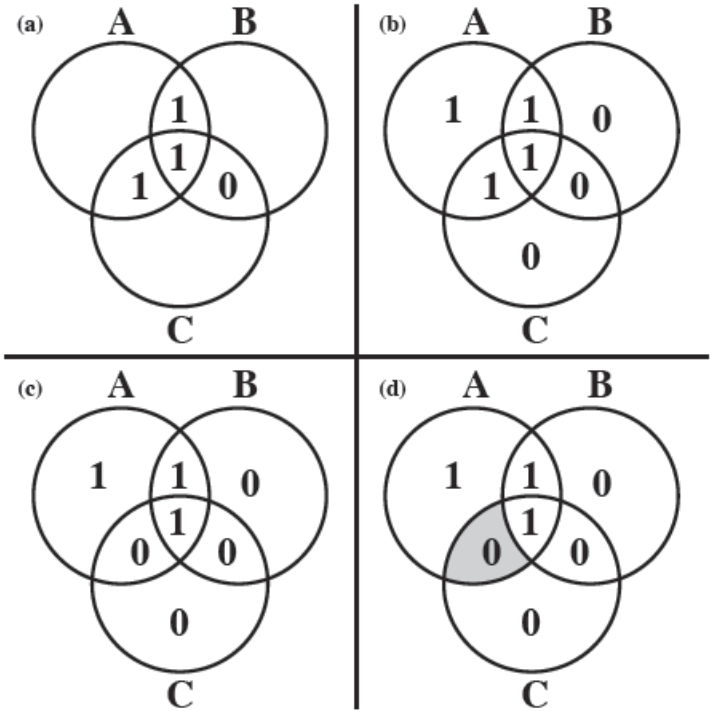


Figure 5.8 Hamming Error-Correcting Code

An error in M data bits can be corrected by using k check bits. From this it is possible to derive the equation $2^k - 1 \geq M + K$. **There are M + K bit positions and if K = 0 then there is no error. With K bits we can denote 2^K things. Since one of these indicates the "no error" condition the remaining 2^K-1 bits must be greater than or equal to the M + K positions.**

Advanced DRAM

SDRAM is **Synchronous DRAM. Synchronized to an external clock and exchanges information with the processor without wait states.**

SDRAM employs a burst mode to improve speed. **SDRAM sends consecutive memory locations at one time thereby eliminating multiple consecutive addresses.**

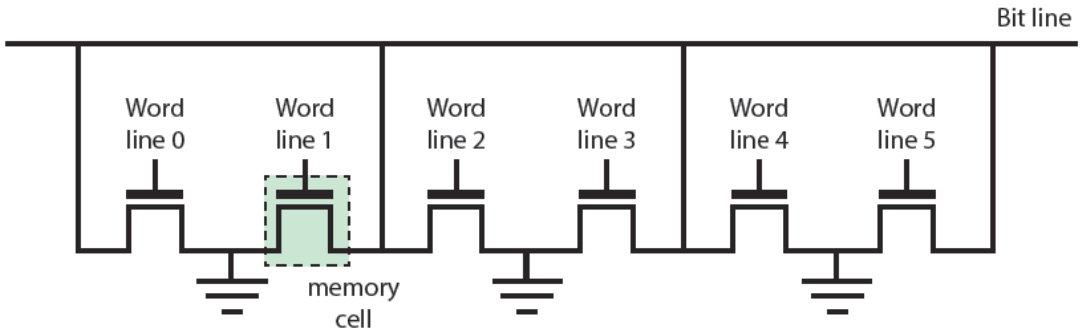
DDR-SDRAM is **Double Data Rate SDRAM. It can send data at twice the clock rate. Effectively breaks RAM organization into two banks and fetches two banks in parallel. It then serializes the data to send it out. It typically uses a rising edge of a clock to fetch data from one bank and a falling edge to fetch data from the second bank.**

Flash Memory

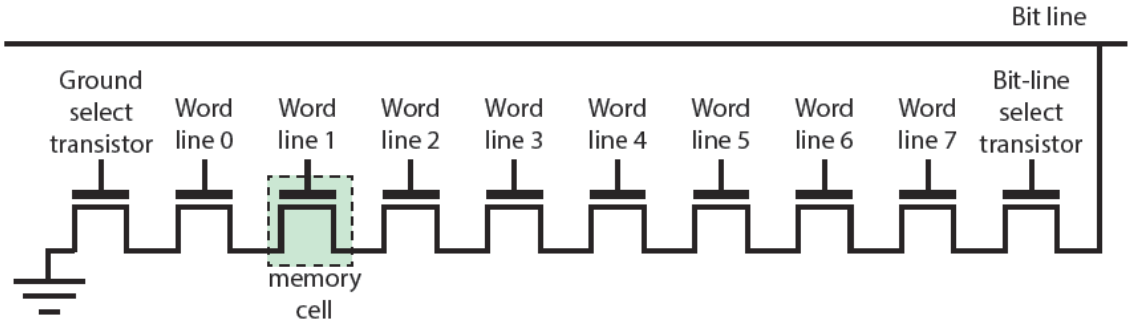
- **Flash memory is named *Flash* because an entire section of memory is erased simultaneously (in a flash).**
- **It uses only 1 transistor per bit and has a similar density to EPROM and EEPROM.**
- **Uses electrical erase technology like EEPROM.**
- **Between EPROM and EEPROM in term of cost and functionality.**

Flash memory works by trapping c**harge in an oxide layer that holds a transistor either on or off permanently.**

There are two types of Flash memory – NAND and NOR flash.



(a) NOR flash structure



(b) NAND flash structure

For the NOR strategy any bit can be selected to allow a bit line to be activated in reading a cell.

For the NAND strategy all of the word lines in the group are turned on making the transistor conduct except for the one being read. You get an output only if the word being read is programmed. The key to understanding this is that you can turn the transistor on without programming them.

USB drive **usually uses NAND flash since it is a little cheaper but not quite as fast since it is harder to access a bit.**

Most Microcontrollers have Flash ROM on them. **This is usually NOR flash since it can be accessed one bit at a time and is a little faster.**

There seems to be something new in memory technology every 6-months to a year. As these new technologies develop they typically fail to compete with existing technologies because the existing technologies are also improving. The author list three new non-volatile RAM technologies that are in production and have promise. They are:
STT-RAM, PCRAM, and ReRAM.
STT-RAM is **Spin-Transfer Torque RAM. A type of magnetic memory that has reading and writing speeds below 10 ns so it is competitive to SRAM. May replace some cache or main memory. Has zero power stand by.**

PCRAM is **Phase-change RAM. This is a magic material which can change state from amorphous to crystalline very fast and does so in response to heating by an electric current. This could replace DRAM.**

ReRAM is **Resistive RAM. This uses a material which changes resistance when a current passes through it thus providing memory. ReRAM is superior to Flash in many ways and may be used for secondary storage.**