Verilog Example with non blocking equals

Given below are two modules which implement a linear feedback shift register (lfsr). Each module has 3 flip-flops which form the shift register with outputs Q[2], Q[1], and Q[0]. The signal called L is the load signal and R is the load value.

One of the modules is implemented with a nonblocking equals and the other uses the blocking equals. Draw the circuit diagram for each module.

Non-blocking Module

module lfsr(R, L, Clock, Q);
    input [2:0] R;
    input L, Clock;
    output [2:0] Q;
    reg [2:0] Q;
    always @(posedge Clock)
        if (L)
            Q <= R;
        else
            Q <= {Q[0], Q[2]^Q[0], Q[1]};
endmodule

Blocking Module

module lfsr(R, L, Clock, Q);
    input [2:0] R;
    input L, Clock;
    output [2:0] Q;
    reg [2:0] Q;
    always @(posedge Clock)
        if (L)
            Q <= R;
        else
            begin
                Q[2] = Q[0];
                Q[1] = Q[2]^Q[0];
                Q[0] = Q[1];
            end
endmodule