1. Design a circuit which will take in a 4-bit binary number, convert this to BCD, and output two 4-bit BCD numbers.

2. Implement the following function using only a 3-8 decoder with active low outputs and NAND gates.

\[ F = \overline{A} \cdot B \cdot C + \overline{B} \]

3. Show how to implement a 5:32 line decoder using 3:8 line decoders.

4. What size ROM would be needed to implement each of the following:
   A) an 8-bit adder/subtractor with Cin and Cout.
   B) a binary multiplier to multiply two 8-bit numbers
   C) A code converter which converts binary to BCD and has a 4-digit BCD output.

5. Draw the PLA circuit which implements the following

\[ F = \sum m(2,3,4,5,6) \]