Counter example

This example illustrates how to set up a clock on the DeoNano board and implement a simple counter. It is assumed that you have read and understand the FPGA Notes.

Create a new project for the DeoNano board that uses the following Verilog code:

```verilog
module CountUpDown(state, a, b, CLOCK_50);
    input a, b;
    input CLOCK_50;
    output state;
    reg [3:0] state;
    reg [31:0] cntDown;
    always @(posedge CLOCK_50)
        begin
            cntDown = cntDown - 1;
        end
    always @(posedge cntDown[25])
        begin
            if(a == 0)
                state = state + 1;
            else if(b == 0)
                state = state - 1;
        end
endmodule
```

In this code the signal CLOCK_50 is a 50 MHz clock that is available on pin r8 on the DeoNano board. The variable cntDown is a 32 bit down counter. The second always block in the Verilog code uses bit 25 of this counter to clock a four bit counter called "state". If button a is pushed the counter counts up. If button b is pushed the counter counts down. If neither button is pushed nothing is done.

Refer to page 11 of the FPGA notes to get the pin assignments for the push buttons, LEDs and CLOCK_50.