Design and implement a sequence detector which will recognize the three-bit sequence 110. Your detector should output a 1 each time the sequence 110 comes in. The input is a clocked serial bit stream.

Mealy Machine

Figure 1 shows a state diagram for a Mealy machine version of the detector.

The corresponding state table is shown in Figure 2.

Figure 2
State table for the sequence detector.

Figure 3 shows the K-maps corresponding to the state table with the equations for the D-type flip-flops.

Figure 3
K-maps and equations for implementation with D-type flip-flops
Figure 4
Implementation with D-type flip-flops.

//Sequence110.v
//Recognizes the sequence 110
module sequence110(clk, dIn, dOut);
  input clk;
  input dIn;
  output dOut;
  reg Qa, Qb;
  wire dA, dB, dOut;
  assign dA = dIn & (Qa | Qb);
  assign dB = dIn & ~Qa & ~Qb;
  assign dOut = ~dIn & Qa;
  always @(posedge clk)
    begin
      Qa <= dA;
      Qb <= dB;
    end
endmodule

Figure 5
Verilog implementation. Note that D_B is implemented as $D_{in} \cdot \overline{A} \cdot \overline{B} = D_{in} \cdot (A + B)$.

Figure 6
Simulation results from Verilog code.

Rework this problem as the equivalent Moore machine.