1. Suppose we make the following declarations:
   wire[3:1] w;
   wire w1;
   wire [1:0] w2;

   Determine whether each of the following is legal or illegal and if illegal state why.
   A) w1 = w[2]; _______________________
   B) w2 = w[1:0]; _______________________
   C) w2 = w[1:2]; _______________________

2. In Verilog the parameter keyword is used to declare ____________.

3. Draw the schematic for the following Verilog code.
   module mystery1(f, s1, s0, i3, i2, i1, i0);
   input s1, s0, i3, i2, i1, i0;
   output f;
   not(ns1, s1);
   not(ns0, s0);
   and(a3, i3, s1, s0);
   and(a2, i2, s1, ns0);
   and(a1, i1, ns1, s0);
   and(a0, i0, ns1, ns0);
   or(f, a3, a2, a1, a0);
   endmodule

4. Rewrite the Verilog code for problem 3 using only the bit wise operators.

5. Draw the schematic for the following Verilog code.
   module mystery2(s, c, x, y, z);
   input x, y, z;
   output s, c;
   assign {c, s} = x + y + z;
   endmodule

6. What value is output to f when the following module is executed if a = 0, b = 1, and c = 0.
   module(f, a, b, c);
   input a, b, c;
   output f;
   wire w;
   f = (a & b) | c;
   assign c = 'b1;
   assign w = c & b;
   endmodule
7. A 4-bit priority encoder has four inputs a0, a1, a2, and a3, and three outputs n1, n0, and r. If all of the inputs are 0 then r = 0 indicating that nothing is encoded else r = 1. The outputs n1 and n0 form a two bit number giving the number of the input which is on and has the highest priority. A truth table is shown below.

<table>
<thead>
<tr>
<th>A0</th>
<th>A1</th>
<th>A2</th>
<th>A3</th>
<th>N1</th>
<th>N0</th>
<th>r</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>x</td>
<td>x</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>x</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>x</td>
<td>x</td>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>x</td>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Truth table for a 4-bit priority encoder.

Fill in the following K-maps for the three outputs, write the function for each output, and write the Verilog implementation.