1T-SRAM-Q™: Quad-Density Technology Reins in Spiraling Memory Requirements

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Introduction

For system-on-chip (SoC) designers, memory-intensive applications in communications, graphics and personal electronics continue to accelerate the need for larger, faster embedded memory arrays in more complex SoC devices. Already, the memory content of typical SoCs has grown to replace logic as the largest component of these highly integrated devices – and memory content will heavily dominate logic within a few years. Accordingly, embedded memory continues to exert the largest influence on SoC yield, cost, speed and reliability. By taking advantage of evolutionary trends in memory technology, however, designers can substantially improve cost, quality and performance of SoCs comprising great numbers of large memory blocks. With the introduction of 1T-SRAM-Q technology, MoSys extends its silicon-proven 1T-SRAM® memory with a high-density memory solution based on an innovative, scalable bit cell capacitor technology that enables very large memory arrays with 4x the density of traditional six-transistor (6T) SRAM.

Evolving Requirements

Unrelenting demand for improved memory has fueled research into a diverse array of alternative memory technologies. Over the past several decades, however, most novel approaches failed the leap from laboratory to production due to their need for costly manufacturing processes and mismatched models of cost and benefit. Indeed, among the myriad of proposed technologies, traditional DRAM and 6T SRAM have endured – and flourished – because of their manufacturing advantages and device benefits. With the popular emergence of SoC designs in the 1990s, however, attempts to force these traditional technologies to meet growing needs for density and logic integration have left designers with few effective alternatives. While DRAM requires significant process changes for logic integration, 6T SRAM lacks the capability to deliver dramatic improvements in density, reliability and low power at a low cost. Despite these limitations, designers accepted these familiar technologies – and their fundamental compromises in density, cost and performance.

Driven by emerging data-intensive applications, memory density started to become a more significant issue for SoC design in the late 1990s. By 1999, memory accounted for 20 percent of SoC area, according to the Semiconductor Industry Association's International Technology Roadmap for Semiconductors (ITRS). At this level, however, designers could no longer justify limitations and compromises associated with traditional memory architectures. Increasingly, designers needed embedded memory architecture able to deliver substantially improved density – all while preserving compatibility with mainstream manufacturing technologies and system-level interfaces. In this environment, MoSys introduced its first-generation 1T-SRAM architecture, delivering twice the density of 6T SRAM while using standard CMOS logic processes – and providing a foundation for evolutionary solutions to meet rising SoC embedded memory requirements.

1T-SRAM®: First-Generation Memory for High-Density Applications

With its introduction of 1T-SRAM technology in 1998, MoSys responded to growing demand in the late 1990s for high density embedded memory. Unlike alternative approaches, 1T-SRAM technology was unique in offering a high-density embedded memory solution built on standard CMOS logic processes.

1T-SRAM memory broke new ground with its one-transistor, one-capacitor bit cell that is 2x smaller than conventional 6T memory and 50 to 70 percent lower in cost. With its smaller size, the 1T-SRAM bit cell features bit lines and word lines that are not only substantially shorter than those in 6T cells but also use metal layers rather than polysilicon to further boost performance and lower power consumption – by as much as 75 percent compared to 6T memories. Besides improving yield through its smaller size, 1T-SRAM memory's use of standard logic design rules further enhances yield compared to 6T SRAM technologies and their aggressive design rules.

While 1T-SRAM technology maintains manufacturing compatibility through its use of standard logic processes, 1T-SRAM memories themselves maintain system-level compatibility through use of a familiar SRAM interface, featuring refresh-free, single-cycle operation for maximum data throughput. With MoSys' patented MultiBank® architecture, the 1T-SRAM architecture partitions memory into large numbers of small banks. During each bank's normal idle cycles, internal refresh management circuitry ensures that each cell's capacitor retains its charge by performing refresh operations that occur transparently in the background, independent of the system interface and without affecting read or write cycles. Even banks that are accessed for prolonged periods can nevertheless refresh thanks to a unique caching scheme that ensures periodic idle cycles even for those active banks. The result is a memory architecture that combines very fast random cycle performance and low power consumption with full compatibility of standard logic processes for optimum yield in embedded applications.

1T-SRAM-M™: Second-Generation Memory for Low-Power Applications

As demand grew sharply at the beginning of the decade for more sophisticated mobile applications, SoC designers faced increased need for lower power embedded memory solutions. Even with rising memory sizes, SoC designers need the ability to reduce power in standby mode to maximize battery life in cell phones, handheld computers and other memory-intensive mobile appliances.

Introduced in 2001, 1T-SRAM-M technology delivers dramatically lower standby power characteristics. Based on the 1T-SRAM architecture, 1T-SRAM-M features unique leakage suppression circuitry that achieves standby current as low as 10µA/Mbit with full data retention. As with its underlying 1T-SRAM technology, 1T-SRAM-M uses standard logic processes, combining high yield, density and performance with reduced standby power requirements needed for evolving mobile applications.

1T-SRAM-R™: Third-Generation Memory for High-Reliability Applications

With designers adding more blocks comprising larger memory arrays to SoCs, embedded memory has already grown to become the largest single component of these complex devices. Accordingly, in driving the quality of the SoC itself, the quality of embedded memory has emerged as a critical issue.

With the introduction of 1T-SRAM-R in 2002, MoSys delivered a next-generation architecture designed to enhance quality across the product

life cycle – with improved yield during manufacturing, improved reliability after manufacturing and enhanced soft error rate (SER) during product use.

With 1T-SRAM-R, MoSys augmented the basic 1T-SRAM architecture with an enhanced reliability option called Transparent Error Correction™ (TEC™) – a MoSys patented technology that eliminates the need for costly repair during manufacture or slow self-repair at power-up.

Unlike conventional redundancy-based repair approaches, TEC dynamically repairs errors during manufacturing, avoiding the additional manufacturing costs and delays associated with laser repair during production. Furthermore, TEC dynamically repairs errors during use, providing SER under 10 FITs/Mbit – 1,000x less than that of 6T SRAM. While conventional ECC approaches add 20 to 30 percent more area for additional redundant memory bits, TEC adds essentially no additional area: Although it uses 20 percent more bit cells, its bit cells are 20 percent smaller than even 1T-SRAM cells. By enhancing quality without silicon overhead, 1T-SRAM-R addresses growing concerns about the impact of large embedded memories on SoC yield, reliability and soft error rates.

1T-SRAM-Q™: Fourth-Generation Memory for Highest-Density Memory

Today, evolving applications in consumer and communications products are routinely boosting memory requirements to new levels. Indeed, memory is directly tied to product differentiation in products like imaging products, where the desire for higher resolution translates into larger memory arrays for frame buffers in digital camcorders, for example. Similarly, demand for higher resolution graphics in lower cost consumer products drive manufacturers to find ways to reduce system complexity and parts count – using highly integrated devices with denser embedded memory arrays to replace separate SRAM chips.
In the face of this application demand, memory content of SoC designs has accelerated dramatically, and in 2002, memory content of SoCs for the first time surpassed SoC logic content. Furthermore, memory will continue to dominate SoCs, according to the ITRS roadmap, reaching 71 percent in 2005 and 94 percent in 2014 (*Figure 1*).

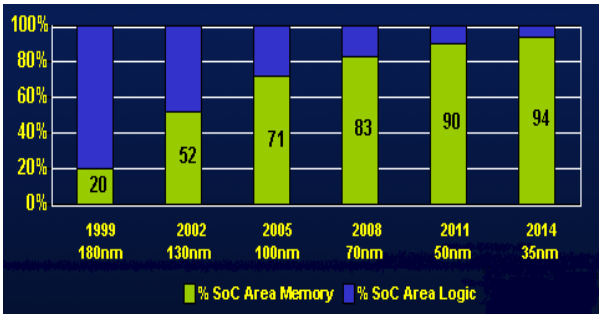

Figure 1. Increase in memory content with migration to advanced process technologies.

As memory consumes more SoC silicon area, concerns about memory density take on a new urgency. Encompassing over 50 percent of SoC area at the end of 2002, memory has more than reached the point where significantly denser memory solutions are needed. Today, SoC manufacturers need a breakthrough in density to help reduce spiraling SoC costs and meet skyrocketing memory demands in the near future. MoSys has achieved this breakthrough with its 1T-SRAM-Q memory, a new memory technology that achieves 4x the density of 6T SRAM while providing excellent scalability to future nanometer nodes (*Table 1*).

1T-SRAM-Q memory represents the fourth generation in the evolution of 1T-SRAM memory technology.

While earlier generations provided key features needed to meet prevailing application requirements, 1T-SRAM-Q memory represents an important evolutionary step in bit cell technology. Using an innovative capacitor technology, called Folded Area Capacitor™ (FAC™) technology, 1T-SRAM-Q memory provides a very high-density embedded memory solution, requiring only an additional non-critical mask and two simple steps that exert no adverse affects on logic.

With this technology, SoC designers can begin to achieve true system-level memory solutions, incorporating arrays of over 128 Mb at 0.13 µm and over 256 Mb at 90 nm. At these memory sizes, designers can integrate main memory on SoCs, reducing external chip count while speeding overall application performance and system reliability.

Based on the same one-transistor, one-capacitor architecture, 1T-SRAM-Q memory incorporates all the features of 1T-SRAM technology, including the MultiBank architecture and circuitry for hidden refresh. Although the smaller 1T-SRAM-Q bit cell inherently offers improved SER characteristics, 1T-SRAM-Q technology also incorporates TEC. Introduced earlier in 1T-SRAM-R technology, TEC provides its significant quality enhancements to large 1T-SRAM-Q memory arrays – and to memory-dominated SoCs. In addition, designers can optionally include the low-power design features of 1T-SRAM-M technology to support improved battery life in memory-intensive mobile applications.

By exploiting the advances made available with each generation of 1T-SRAM technology, 1T-SRAM-Q memory provides designers with a memory architecture that combines extremely high density, high reliability and low-power options. With FAC technology, however, 1T-SRAM-Q technology inherently provides key performance enhancements over the previous generations of 1T-SRAM technology – and dramatic improvements over traditional 6T SRAM technology.

1T-SRAM-Q Performance

Built vertically in the bit cell, the 1T-SRAM-Q capacitor retains the same bit-cell capacitance as in 1T-SRAM memory, but within a substantially smaller bit cell. In memory technology, smaller means faster timing and lower power operation, because operating characteristics can scale down with the smaller bit cell. A smaller cell means shorter metal bit lines, which translates to reduced parasitics. In turn, reduced parasitics enable faster timing and higher performance.

Besides shorter metal bit lines, 1T-SRAM-Q memory's shorter metal word lines mean faster charging and discharging – and faster read and write cycles. In fact, while 1T-SRAM technology has provided 40%-50% speed improvements at each succeeding technology node, these factors enable 1T-SRAM-Q memory to offer a 10 to 20 percent speed improvement over 1T-SRAM memory at the same process node.

	0.25µm	0.18µm	0.13µm	90nm	65nm	45nm
1T-SRAM-Q™						
Macro (mm²/Mbit)			*1.05*	*0.55*	*0.29*	*0.14*
Bitcell (µm²)			*0.50*	*0.28*	*0.15*	*0.07*
1T-SRAM®						
Macro (mm²/Mbit)	*7.0*	*3.6*	*1.9*	*1.1*	*0.57*	*0.28*
Bitcell (µm²)	*3.51*	*1.97*	*1.10*	*0.61*	*0.32*	*0.15*
6T SRAM						
Macro (mm²/Mbit)	*11.28*	*7.18*	*3.73*	*2.09*	*1.09*	*0.52*
Bitcell (µm²)	*7.56*	*4.65*	*2.43*	*1.36*	*0.71*	*0.34*

Table 1. Comparison of cell size for 1T-SRAM-Q, 1T-SRAM and 6T SRAM technologies.

In fact, 1T-SRAM-Q technology offers another fundamental advantage in signal integrity, which can also lead to further memory enhancements. The 1T-SRAM-Q capacitor provides about the same charge storage as the 1T-SRAM capacitor. Because its bit cell is 2x smaller than the 1T-SRAM cell, however, 1T-SRAM-Q technology provides an improved ratio of stored charge to parasitics, resulting in an improved signal-to-noise ratio (SNR).

Typically, high-density designs face tighter signal margins as voltages drop in more advanced process technologies at 90 nm and below.

With its improved SNR, however, 1T-SRAM-Q can take advantage of additional available timing margin to speed performance or increase reliability for applications that do not require clock rates at the edge of the envelope.

The favorable ratio of charge to bit cell circuitry also translates directly into reduced power-dissipation characteristics for 1T-SRAM-Q memories. Shorter wires, fewer parasitics and lower voltage combine to reduce 1T-SRAM-Q memory's dynamic power requirements without impacting speed or reliability.

1T-SRAM-Q Technology Innovations

1T-SRAM-Q's advantages spring from the use of a new, highly efficient capacitor technology that stretches vertically in the 1T-SRAM-Q cell, rather than horizontally as in the 1T-SRAM cell *(Figure 2*).
Using an additional mask, the 1T-SRAM-Q fabrication process uses two extra steps to etch a well in the shallow trench isolation (STI) layer and fill it with polysilicon.
Oxide forms naturally, bending from the horizontal plate down into the well (*Figure 3*), creating the 1T-SRAM-1T-SRAM-Q's Folded Area Capacitor. The FAC well reaches deep into the STI layer, providing a robust capacitor structure that retains a large effective area – and charge – even as the bit cell is scaled down to more advanced technology nodes at 65 nm and 45 nm.

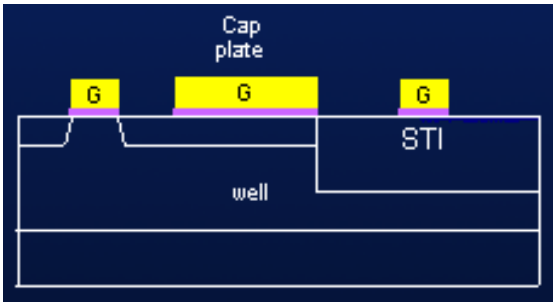

Figure 2. 1T-SRAM cross section showing horizontal capacitor plate.

The additional etch and implant steps occur before transistors are fabricated, so this approach introduces no extra thermal cycles. In contrast, embedded DRAM requires process changes that cause additional thermal cycles. These additional heating and cooling passages affect the characteristics of the logic transistors. As a result, embedded DRAM processes are inevitably different from standard logic processes, and logic transistors produced with embedded DRAM processes do not have quite the same performance as those produced with standard logic processes. Because 1T-SRAM-Q memory's process does not introduce additional thermal cycles, engineers can be confident that this process does not impact performance of the rest of the chip. Furthermore, the 1T-SRAM-Q process does not result in any adverse topography, because the no FAC structures rise above the plane to affect layers placed above it.

Fabricating the FAC requires only an additional mask that is non-critical – and therefore relatively inexpensive. With two additional steps, 1T-SRAM-Q technology increases manufacturing cost by about 5%. On the other hand, 1T-SRAM-Q technology reduces memory

array size by a factor of two compared with the next best alternative, 1T-SRAM memory.

Consequently, for a typical SoC comprising 50 percent memory, the use of 1T-SRAM-Q technology typically returns a 25 percent cost improvement at only a five percent increment in manufacturing cost – a favorable cost model that holds true for SoCs with memory content as low as 10 percent. For much smaller partitions below 0.25 Mb, the incremental size disadvantage of conventional 6T SRAM is negligible, justifying its use for very small arrays. Between these boundaries, first-generation 1T-SRAM technology provides a cost-effective solution (*Figure 4*). Beyond this cost overview, MoSys' online memory savings calculator provides a detailed analysis of cost considerations and savings. You can try it free. Just link to the MoSys calculator page at: http://www.mosys.com/products/sv_calc_1.html

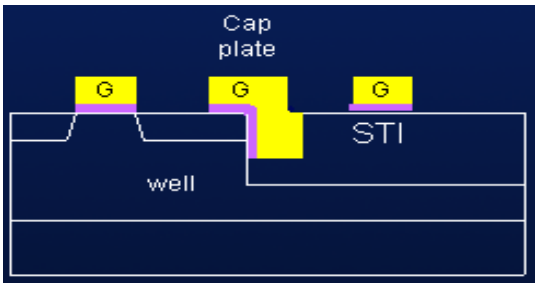

Figure 3. 1T-SRAM-Q cross-section showing vertical capacitor (FAC).

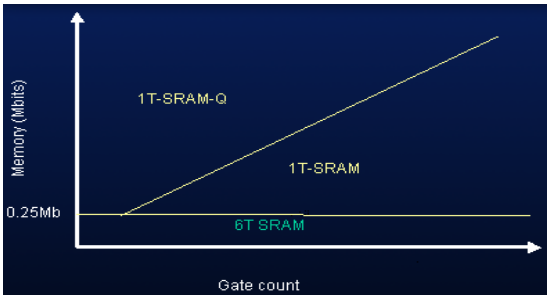

Figure 4. Memory technology selection criteria.

Conclusions

With over 50 million units shipped, the 1T-SRAM family is a production-proven embedded memory solution, able to meet the demand for higher density, reliability and low power. Licensed by market leaders in communications, consumer and graphics segments, 1T-SRAM technology has been repeatedly proven in silicon through five generations of standard CMOS logic processes.

As need grows for dramatic improvements in memory density, 1T-SRAM-Q technology builds on the features of earlier 1T-SRAM generations, leveraging the scalability advantages of FAC technology. With the addition of simple, low-cost steps in standard CMOS logic fabrication, 1T-SRAM-Q technology delivers substantial gains in density, speed and power – providing a cost-effective solution to burgeoning demand for more cost-effective embedded memories in complex SoC devices.

About the Author

Mark-Eric Jones is vice president and general manager - Intellectual Property. Prior to joining the company, Mr. Jones served as director of the Intellectual Property Division at Mentor Graphics Corporation, a developer of EDA tools and provider of intellectual property. Prior, Mr. Jones founded 3Soft, Inc., a developer of intellectual property where he served as president and chief executive officer. Mr. Jones received a master's degree from Trinity College and University of Cambridge, United Kingdom.