Overview: Partial-Scan & Scan Variations

- Definition
- Partial-scan architecture
- Scan flip-flop selection methods
- Cyclic and acyclic structures
- Partial-scan by cycle-breaking
- Scan variations
- Scan-hold flip-flop (SHFF)
- Summary

Partial-Scan Definition

- A subset of flip-flops is scanned.
- Objectives:
  - Minimize area overhead and scan sequence length, yet achieve required fault coverage
  - Exclude selected flip-flops from scan:
    - Improve performance
    - Allow limited scan design rule violations
  - Allow automation:
    - In scan flip-flop selection
    - In test generation
  - Shorter scan sequences

Partial-Scan Architecture

Scan Flip-Flop Selection Methods

- Testability measure based
  - Use of SCOAP: limited success.
- Structure based:
  - Cycle breaking
  - Balanced structure
    - Sometimes requires high scan percentage
- ATPG based:
  - Use of combinational and sequential TG

Cycle Breaking

- Difficulties in ATPG
- S-graph and MFVS problem
- Test generation and test statistics
- Partial vs. full scan
- Partial-scan flip-flop
Difficulties in Seq. ATPG

- Poor initializability.
- Poor controllability/observability of state variables.
- Gate count, number of flip-flops, and sequential depth do not explain the problem.
- Cycles are mainly responsible for complexity.

<table>
<thead>
<tr>
<th>Circuit</th>
<th>Number of gates</th>
<th>Number of flip-flops</th>
<th>Sequential depth</th>
<th>ATPG CPU s</th>
<th>Fault coverage</th>
</tr>
</thead>
<tbody>
<tr>
<td>TLC</td>
<td>355</td>
<td>21</td>
<td>14</td>
<td>1,247</td>
<td>99.01%</td>
</tr>
<tr>
<td>Chip A</td>
<td>1,112</td>
<td>30</td>
<td>14</td>
<td>260</td>
<td>98.80%</td>
</tr>
</tbody>
</table>

* Maximum number of flip-flops on a PI to PO path

Benchmark Circuits

<table>
<thead>
<tr>
<th>Circuit</th>
<th>TLC</th>
<th>Chip A</th>
<th>ABC</th>
<th>DEF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of gates</td>
<td>355</td>
<td>1,112</td>
<td>100</td>
<td>150</td>
</tr>
<tr>
<td>Number of flip-flops</td>
<td>21</td>
<td>30</td>
<td>20</td>
<td>25</td>
</tr>
<tr>
<td>Sequential depth</td>
<td>14</td>
<td>14</td>
<td>14</td>
<td>14</td>
</tr>
<tr>
<td>ATPG CPU s</td>
<td>1,247</td>
<td>260</td>
<td>89.01%</td>
<td>98.80%</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>99.01%</td>
<td>98.80%</td>
<td>89.01%</td>
<td>98.80%</td>
</tr>
</tbody>
</table>

Cycle-Free Example

All faults are testable. See Example 8.6.

A Partial-Scan Method

- Select a minimal set of flip-flops for scan to eliminate all cycles.
- Alternatively, to keep the overhead low only long cycles may be eliminated.
- In some circuits with a large number of self-loops, all cycles other than self-loops may be eliminated.

The MFVS Problem

- For a directed graph find a set of vertices with smallest cardinality such that the deletion of this vertex-set makes the graph acyclic.
- The minimum feedback vertex set (MFVS) problem is NP-complete; practical solutions use heuristics.
- A secondary objective of minimizing the depth of acyclic graph is useful.
Test Generation

- Scan and non-scan flip-flops are controlled from separate clock PIs:
  - Normal mode – Both clocks active
  - Scan mode – Only scan clock active
- Seq. ATPG model:
  - Scan flip-flops replaced by PI and PO
  - Seq. ATPG program used for test generation
  - Scan register test sequence, 001100…, of length \( n_{\text{ATPG}} + 4 \) applied in the scan mode
  - Each ATPG vector is preceded by a scan-in sequence to set scan flip-flop states
  - A scan-out sequence is added at the end of each vector sequence
- Test length = \( (n_{\text{ATPG}} + 2)n_{\text{eff}} + n_{\text{ATPG}} + 4 \) clocks

Partial Scan Example

- Circuit: TLC
- 355 gates
- 21 flip-flops

<table>
<thead>
<tr>
<th>Scan flip-flops</th>
<th>Max. cycle length</th>
<th>Depth</th>
<th>ATPG</th>
<th>CPU s</th>
<th>Fault sim.</th>
<th>Fault</th>
<th>ATPG vectors</th>
<th>Test seq. length</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>4</td>
<td>14</td>
<td>1247</td>
<td>61</td>
<td>89.01%</td>
<td>805</td>
<td>805</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>2</td>
<td>10</td>
<td>137</td>
<td>11</td>
<td>95.50%</td>
<td>247</td>
<td>1,249</td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>5</td>
<td>32</td>
<td>4</td>
<td>99.20%</td>
<td>136</td>
<td>1,382</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>3</td>
<td>13</td>
<td>4</td>
<td>100.00%</td>
<td>112</td>
<td>1,256</td>
<td></td>
</tr>
<tr>
<td>21</td>
<td>0</td>
<td>0</td>
<td>2</td>
<td>2</td>
<td>100.00%</td>
<td>52</td>
<td>1,190</td>
<td></td>
</tr>
</tbody>
</table>

* Cyclic paths ignored

Partial vs. Full Scan: S5378

<table>
<thead>
<tr>
<th>Partial-scan</th>
<th>Full-scan</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of combinational gates</td>
<td>2,781</td>
</tr>
<tr>
<td>Number of non-scan flip-flops (10 gates each)</td>
<td>179</td>
</tr>
<tr>
<td>Number of scan flip-flops (14 gates each)</td>
<td>0</td>
</tr>
<tr>
<td>Gate overhead (14 gates each)</td>
<td>0.0%</td>
</tr>
<tr>
<td>Number of faults</td>
<td>4,603</td>
</tr>
<tr>
<td>ATPG for SFF</td>
<td>2,781</td>
</tr>
<tr>
<td>Fault coverage</td>
<td>99.9%</td>
</tr>
<tr>
<td>Fault efficiency</td>
<td>99.9%</td>
</tr>
<tr>
<td>CPU time on SUN Ultra II</td>
<td>5,533 s</td>
</tr>
<tr>
<td>Number of ATEP vectors</td>
<td>414</td>
</tr>
<tr>
<td>Scan sequence length</td>
<td>1,117</td>
</tr>
</tbody>
</table>

Flip-flop for Partial Scan

- Normal scan flip-flop (SFF) with multiplexer of the LSSD flip-flop is used.
- Scan flip-flops require a separate clock control:
  - Either use a separate clock pin
  - Or use an alternative design for a single clock pin

Scan Variations

- Integrated and Isolated scan methods
  - Scan path: NEC 1968
  - Serial scan: 1973
  - LSSD: IBM 1977
  - Scan set: Univac 1977
  - RAS: Fujitsu/Amdahl 1980

Scan Set
Scan Set Applications

- Advantages
  - Potentially useable in delay testing.
  - Concurrent testing: can sample the system state while the system is running
    • Used in microrollback
- Disadvantages
  - Higher overhead due to routing difficulties

Random-Access Scan (RAS)

RAS Flip-Flop (RAM Cell)

RAS Applications

- Logic test: reduced test length.
- Delay test: Easy to generate single-input-change (SIC) delay tests.
- Advantage: RAS may be suitable for certain architecture, e.g., where memory is implemented as a RAM block.
- Disadvantages:
  • Not suitable for random logic architecture
  • High overhead – gates added to SFF, address decoder, address register, extra pins and routing

Scan-Hold Flip-Flop (SHFF)

Summary

- Partial-scan is a generalized scan method; scan can vary from 0 to 100%.
- Elimination of long cycles can improve testability via sequential ATPG.
- Elimination of all cycles and self-loops allows combinational ATPG.
- Partial-scan has lower overheads (area and delay) and reduced test length.
- Partial-scan allows limited violations of scan design rules, e.g., a flip-flop on a critical path may not be scanned.