Overview

Major ATPG algorithms
- Definitions
  - D-Algorithm (Roth) -- 1966
    - D-cubes
    - Bridging faults
    - Logic gate function change faults
  - PODEM (Goel) -- 1981
    - X-Path-Check
    - Backtracing
- Summary

Forward Implication
- Results in logic gate inputs that are significantly labeled so that output is uniquely determined
- AND gate forward implication table:

\[
\begin{array}{ccc}
D & 0 & 1 \\
0 & 0 & 0 & 0 & 0 \\
1 & 0 & 0 & 0 & 0 \\
X & 0 & 1 & X & D \\
D & 0 & D & X & 0 \\
D & 0 & D & X & D \\
\end{array}
\]

Backward Implication
- Unique determination of all gate inputs when the gate output and some of the inputs are given

Objectives and Backtracing in ATPG
- **Objective** – desired signal value goal for ATPG
  - Guides it away from infeasible/hard solutions
  - Uses heuristics
- **Backtrace** – Determines which primary input and value to set to achieve objective
  - Use heuristics such as nearest PI
- **Forward trace** – Determines gate through which the fault effect should be sensitized
  - Use heuristics such as output that is closest to the present fault effect
Branch-and-Bound Search

- Efficiently searches binary search tree
- Branching – At each tree level, selects which input variable to set to what value
- Bounding – Avoids exploring large tree portions by artificially restricting search decision choices
  - Complete exploration is impractical
  - Uses heuristics

D-Algorithm – Roth (1966)

- Fundamental concepts invented:
  - First complete ATPG algorithm
  - D-Cube
  - D-Calculus
  - Implications – forward and backward
  - Implication stack
  - Backtrack
  - Test Search Space

Singular Cover Example

- Minimal set of logic signal assignments to represent a function
  - show prime implicants and prime implicants of Karnaugh map (with explicitly showing the outputs too)

Gate Inputs Output | Gate Inputs Output
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>AND A B d</td>
<td>NOR d e f</td>
</tr>
<tr>
<td>1 0 X 0 1 1 X 0</td>
<td></td>
</tr>
<tr>
<td>2 X 0 0 2 X 1 0</td>
<td></td>
</tr>
<tr>
<td>3 1 1 1 3 0 0 1</td>
<td></td>
</tr>
</tbody>
</table>

Primitive D-Cube of Failure

- Models circuit faults:
  - Stuck-at-0
  - Stuck-at-1
  - Other faults, such as Bridging fault (short circuit)
  - Arbitrary change in logic function
- AND Output sa0: “1 1 D”
- AND Output sa1: “0 X D”
- Wire sa0: “X D”
- Propagation D-cube – models conditions under which fault effect propagates through gate

Construction of Primitive D-Cubes of Failure

1. Make cube set $\alpha_1$ when good machine output is 1 and set $\alpha_0$ when good machine output is 0
2. Make cube set $\beta_1$ when failing machine output is 1 and $\beta_0$ when it is 0
3. Change $\alpha_1$ outputs to 0 and D-intersect each cube with every $\beta 0$. If intersection works, change output of cube to D
4. Change $\alpha_0$ outputs to 1 and D-intersect each cube with every $\beta 1$. If intersection works, change output of cube to D

Gate Function Change D-Cube of Failure

<table>
<thead>
<tr>
<th>Cube-set a b c</th>
<th>Cube-set a b c</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\alpha 0$ 0 X 0 PFDs for AND changing to OR</td>
<td>0 1 D</td>
</tr>
<tr>
<td>X 0 0</td>
<td>1 0 D</td>
</tr>
<tr>
<td>$\alpha 1$ 1 1</td>
<td>1 X 1</td>
</tr>
<tr>
<td>$\beta 0$ 0 0</td>
<td>X 1 1</td>
</tr>
<tr>
<td>$\beta 1$ 1 X 1</td>
<td>X 1 1</td>
</tr>
</tbody>
</table>
Propagation D-Cube

• Collapsed truth table entry to characterize logic
• Use Roth’s S-valued algebra
• AND gate: use the rules given earlier using α and β but in this case work with good circuit only

Write all primitive Cubes of AND gate and then create propagation cubes

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>D</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td>D</td>
<td>D</td>
<td>D</td>
<td>D</td>
</tr>
</tbody>
</table>

D-Cube Operation of D-Intersection

ψ – undefined (same as φ)
μ or λ – requires inversion of D and \( \overline{D} \)

- **D-intersection:** \( 0 \lor 0 = 0 \lor \overline{X} = \overline{X} \lor 0 = 0 \)
- \( 1 \lor 1 = 1 \lor \overline{X} = \overline{X} \lor 1 = 1 \)
- \( X \lor X = X \)

- **D-containment –** Cube \( a \) contains Cube \( b \) if \( b \) is a subset of \( a \)

Implication Procedure

1. Model fault with appropriate primitive D-cube of failure (PDF)
2. Select propagation D-cubes to propagate fault effect to a circuit output (D-drive procedure)
3. Select singular cover cubes to justify internal circuit signals (Consistency procedure)
   - Put signal assignments in test cube
   - Regrettably, cubes are selected very arbitrarily by D-ALG

D-Algorithm – Top Level

1. Number all circuit lines in increasing level order from PIs to POs;
2. Select a primitive D-cube of the fault to be the test cube;
   - Put logic outputs with inputs labeled as D (D) onto the D-frontier;
3. **D-drive**;
4. **Consistency**;
5. return ();

D-Algorithm – D-drive

while (untried fault effects on D-frontier)
  select next untried D-frontier gate for propagation;
  while (untried fault effect fanouts exist)
    select next untried fault effect fanout;
    generate next untried propagation D-cube;
    D-intersect selected cube with test cube;
    if (intersection fails or is undefined) continue;
    if (all propagation D-cubes tried & failed) break;
    if (intersection succeeded)
      add propagation D-cube to test cube – recreate D-frontier;
      Find all forward & backward implications of assignment;
      save D-frontier, algorithm state, test cube, fanouts, fault;
    break;
  else if (intersection fails & D and D in test cube)
    Backtrack ();
    Find all forward & backward implications of assignment, and break;
  else
    **D-drive**;
    if (singular cover D-intersects with \( z \)) delete \( z \) from \( g \), add inputs to singular cover (i.e. find all forward and backward implications of new assignment), and break;
    if (intersection fails) mark singular cover as failed;
Backtrack

if (PO exists with fault effect) Consistency ();
else pop prior implication stack setting to try alternate assignment;
if (no untried choices in implication stack) fault untestable & stop;
else return;

Circuit Example 7.1 and Truth Table

<table>
<thead>
<tr>
<th>Inputs</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>a b c</td>
<td>F</td>
</tr>
<tr>
<td>0 0 0</td>
<td>0</td>
</tr>
<tr>
<td>0 0 1</td>
<td>0</td>
</tr>
<tr>
<td>0 1 0</td>
<td>0</td>
</tr>
<tr>
<td>0 1 1</td>
<td>1</td>
</tr>
<tr>
<td>1 0 0</td>
<td>0</td>
</tr>
<tr>
<td>1 0 1</td>
<td>0</td>
</tr>
<tr>
<td>1 1 0</td>
<td>0</td>
</tr>
<tr>
<td>1 1 1</td>
<td>0</td>
</tr>
</tbody>
</table>

Singular Cover & Propagation D-Cubes

- **Singular cover** – Used for justifying lines
- **Propagation D-cubes** – Conditions under which difference between good/failing machines propagates

Steps for Fault \( d \) \( sa0 \)

<table>
<thead>
<tr>
<th>Step</th>
<th>A B C d e F</th>
<th>Cube type</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>D D D D D D</td>
<td>PDF of AND gate</td>
</tr>
<tr>
<td>2</td>
<td>D D D D D D</td>
<td>Prop. D-cube for NOR</td>
</tr>
<tr>
<td>3</td>
<td>1 1 0</td>
<td>Sing. Cover of NAND</td>
</tr>
</tbody>
</table>

Example 7.3 – Fault \( u \) \( sa1 \)

- **Primitive D-cube of Failure**

Example 7.3 – Step 2 \( u \) \( sa1 \)

- **Propagation D-cube for \( v \)**

(a,b) means that the line has CC0 – a and CC1 – b
Example 7.3 – Step 2 u sa1
• Forward and backward implications

Inconsistent
• \( d = 0 \) and \( m = 1 \) cannot justify \( r = 1 \) (equivalence)
  – Backtrack
  – Remove \( B = 0 \) assignment

Example 7.3 – Backtrack
• Need alternate propagation D-cube for \( \nu \)

Example 7.3 – Step 3 u sa1
• Propagation D-cube for \( \nu \) and implications

Example 7.3 – Step 4 u sa1
• Propagation D-cube for \( Z \) and implications
PODEM -- Goel (1981)

- New concepts introduced:
  - Expand binary decision tree only around primary inputs
  - Use X-PATH-CHECK to test whether D-frontier still there
  - Objectives -- bring ATPG closer to propagating D(1) to PO
  - Backtracing

Motivation

- IBM introduced semiconductor DRAM memory into its mainframes – late 1970’s
- Memory had error correction and translation circuits – improved reliability
  - D-ALG unable to test these circuits
  - Search too undirected
  - Large XOR-gate trees
  - Must set all external inputs to define output
  - Needed a better ATPG tool

PODEM High-Level Flow

1. Assign binary value to unassigned PI
2. Determine implications of all PIs
3. Test Generated? If so, done.
4. Test possible with more assigned PIs? If maybe, go to Step 1
5. Is there untried combination of values on assigned PIs? If not, exit: untestable fault
6. Set untried combination of values on assigned PIs using objectives and backtrace. Then, go to Step 2

Example 7.3 Again

- Select path s – Y for fault propagation

Example 7.3 -- Step 2 s sa1

- Initial objective: Set r to 1 to excite fault

Example 7.3 -- Step 3 s sal

- Backtrace from r
Example 7.3 -- Step 4 $s_{sa1}$

- Set $A = 0$ in implication stack

Example 7.3 -- Step 5 $s_{sa1}$

- Forward implications: $d = 0, X = 1$

Example 7.3 -- Step 6 $s_{sa1}$

- Initial objective: set $r$ to 1

Example 7.3 -- Step 7 $s_{sa1}$

- Backtrace from $r$ again

Example 7.3 -- Step 8 $s_{sa1}$

- Set $B$ to 1. Implications in stack: $A = 0, B = 1$

Example 7.3 -- Step 9 $s_{sa1}$

- Forward implications: $k = 1, m = 0, r = 1, q = 1, Y = 1, s = D, u = D, Y = D, Z = 1$
Backtrack -- Step 10 "sa1"

- X-PATH-CHECK shows paths s → Y and s → u → v → Z blocked (D-frontier disappeared)

Step 11 -- s "sa1"

- Set B = 0 (alternate assignment)

Backtrack -- s "sa1"

- Forward implications: d = 0, X = 1, m = 1, r = 0, s = 1, q = 0, Y = 1, v = 0, Z = 1, Fault not sensitized.

Step 13 -- s "sa1"

- Set A = 1 (alternate assignment)

Step 14 -- s "sa1"

- Backtrace from r again

Step 15 -- s "sa1"

- Set B = 0. Implications in stack: A = 1, B = 0
Backtrack -- s sa1
- Forward implications: $d = 0$, $X = 1$, $m = 1$, $r = 0$.
Conflict: fault not sensitized. Backtrack

Fault Tested -- Step 18 s sa1
- Forward implications: $d = 1$, $m = 1$, $r = 1$, $q = 0$, $s = D$, $v = D$, $X = 0$, $Y = D$

Objective Selection Code

if (gate $g$ is unassigned) return $(g, \overline{V})$
select a gate $P$ from the D-frontier;
select an unassigned input $l$ of $P$;
if (gate $g$ has controlling value)
  $c =$ controlling input value of $g$
else if (0 value easier to get at input of XOR/EQUIV gate)
  $c = 1$
else $c = 0$
return $(l, \overline{V})$;

PODEM Algorithm

while (no fault effect at POs)
if (xpathcheck (D-frontier))
  $(l, v) =$ Objective (fault, $v_{\text{new}}$);
  $(pi, v_{pi}) =$ Backtrace $(l, v)$;
  Implies $(pi, v_{pi})$;
if (PODEM (fault, $v_{\text{fault}}$) == SUCCESS) return (SUCCESS);
$(pi, v_{pi}) =$ Backtrace $(l, v)$;
  Implies $(pi, \overline{V})$;
if (PODEM (fault, $v_{\text{fault}}$) == SUCCESS) return (SUCCESS);
  Implies $(pi, \overline{V})$;
  return (FAILURE);
else if (implication stack exhausted)
  return (FAILURE);
else Backtrace $(l)$;
return (SUCCESS);
Summary
• D-ALG – First complete ATPG algorithm
  – D-Cube
  – D-Calculus
  – Implications – forward and backward
  – Implication stack
  – Backup
• PODEM
  – Expand decision tree only around PIs
  – Use X-PATH-CHECK to see if D-frontier exists
  – Objectives – bring ATPG closer to getting
  D 0 to PO
  – Backtracing

Implication Stack
• Push-down stack. Records:
  – Each signal set in circuit by ATPG
  – Whether alternate signal value already tried
  – Portion of binary search tree already searched

Objectives and Backtracing in ATPG
• Objective – desired signal value goal for ATPG
  – Guides it away from infeasible/hard solutions
  – Uses heuristics
• Backtrace – Determines which primary input and
  value to set to achieve objective
  – Use testability measures

Bridging Fault Circuit
• Short Circuit (Bridging Fault)

Bridging Fault D-Cubes of Failure

<table>
<thead>
<tr>
<th>Cube-set</th>
<th>a</th>
<th>b</th>
<th>a* b*</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>1</td>
<td>X</td>
<td>X</td>
<td>1</td>
</tr>
</tbody>
</table>
Example 7.2 Fault A sa0

- Step 1 – D-Drive – Set A = 1

Step 2 -- Example 7.2

- Step 2 – D-Drive – Set f = 0

Step 3 -- Example 7.2

- Step 3 – D-Drive – Set k = 1

Step 4 -- Example 7.2

- Step 4 – Consistency – Set g = 1

Step 5 -- Example 7.2

- Step 5 – Consistency – f = 0 Already set

Step 6 -- Example 7.2

- Step 6 – Consistency – Set c = 0, Set e = 0
D-Chain Dies -- Example 7.2

- Step 7 - Consistency – Set $B = 0$
- D-Chain dies

Test cube: A, B, C, D, e, f, g, h, k, L

Example 7.3 – Fault $s$ sa1

- Primitive D-cube of Failure

Example 7.3 – Step 2 $s$ sa1

- Propagation D-cube for $v$

Example 7.3 – Step 2 $s$ sa1

- Forward & Backward Implications

Example 7.3 – Step 3 $s$ sa1

- Propagation D-cube for $Z$ – test found!