Homework 1 Solutions

1. (10 points) Draw a fully complementary CMOS circuit which implements the following function:

\[ F(a, b) = \begin{cases} 
1, & \text{if } a > b, \\
0, & \text{if } a \leq b. 
\end{cases} \]

where \( a \) and \( b \) are 2-bit unsigned numbers. Your design should use as few transistors as possible. Assume that the input signals \( a_1, a_0, b_1, \) and \( b_0 \) are available in both inverted and non-inverted form. Excessive number of transistors will be penalized.

Solution: Using Kmaps (This is one solution with minimum # of transistors (12))

\[
F = a_1 b_1' + a_0 b_0' b_1' + a_1 a_0 b_0'
\]

\[
F' = a_1' b_1 + (a_1' + b_1) (a_0' + b_0)
\]
2. (10 points) Show that the current through two transistors in series is equal to the current through a single transistor of twice the length when the transistors are in linear region. Specifically, show that $I_{ds1} = I_{ds2}$ when $V_D < (V_G - V_t)$ and $(V_G > V_t)$ in the figure below:

Solution: Consider the figure on the right. Call the voltage between the two transistors $V_x$. We know that $V_x < V_D$. Consequently, $V_x < V_D < V_G - V_t$ and $V_D - V_x < V_G - V_x - V_t$. Therefore, both transistors are in linear region.

$$I_{ds2} = \beta \left( (V_G - V_t - V_x) (V_D - V_x) - \frac{(V_D - V_x)^2}{2} \right)$$

for upper transistor

$$= \beta \left( (V_G - V_t) V_D - \frac{V_x^2}{2} \right) - \beta \left( (V_G - V_t) V_x - \frac{V_x^2}{2} \right)$$

$$= 2I_{ds1} - I_{ds2}.$$ 

Therefore, $I_{ds1} = I_{ds2}$. 

3. Consider a two-input NOR gate where one input is at 0 V and the other input is at \( V_{in} \). For the p-transistors, assume the upper transistor input is at 0 V and the lower transistor is at \( V_{in} \).

(a) (4 points) Guess the region of operation of the transistors when \( V_{in} = 0 \). Verify:

**Solution:** When \( V_{in} = 0 \), the nMOS is in cutoff. Therefore, no current flows through the transistors in steady-state. The upper pMOS is ON because \( V_{GS} = -V_{DD} < -|V_{ip}| \). If a transistor is ON and no current flows through it, the transistor must be in linear region and its \( V_{DS} \) = 0. Therefore, \( V_{1} = V_{DD} \). Since \( V_{1} = V_{DD}, V_{GS} \) of lower pMOS is also \(-V_{DD}\). Therefore, second pMOS is also ON and by the above reasoning, lower pMOS is in linear region and \( V_{2} = V_{DD} \). \( V_{DS} \) of the nMOS is 0. Therefore, nMOS is cutoff.

(b) (6 points) Determine the range of \( V_{in} \) when both p-transistors are in the linear region. Assume \( \beta_n = 190\mu A/V^2 \), \( \beta_p = 66\mu A/V^2 \), \( V_{in} = 0.59 V \), and \( V_{ip} = -0.74 V \). Feel free to use program of your choice (e.g., Matlab, Mathematica, custom C program) to numerically solve the equations.

**Solution:** We are given that the two pMOS are in linear region. Can the nMOS be in linear region? Suppose it is possible. Then, the following conditions must be satisfied:

\[
\text{nMOS} \quad V_{2} < V_{in} - V_{in}
\]
\[
\text{Lower pMOS} \quad V_{1} - V_{2} > 0 - V_{DD} + |V_{ip}|
\]
\[
\text{Upper pMOS} \quad V_{1} - V_{DD} > 0 - V_{DD} + |V_{ip}|
\]

From the first two conditions, \( V_{1} + |V_{ip}| < V_{2} < V_{in} - V_{in} \). This is not possible. Therefore, nMOS cannot be in linear region.

From the solution to part (a), we know that both pMOS are in linear region when \( V_{in} = 0 \). What is the largest \( V_{in} \) for which both pMOS are in linear region. As long as nMOS is in cutoff, the two pMOS are in linear region by the same reasoning as in part (a). That is, pMOS will get out of linear region only when \( V_{in} > V_{in} \) and nMOS is in saturation. The upper pMOS will always be in linear region (irrespective of \( V_{in} \)) because

\[ V_{1} - V_{DD} > 0 - V_{DD} + |V_{ip}| \Rightarrow V_{1} > -|V_{ip}|, \]

which is always true. Therefore, we are interested in the largest \( V_{in} \) when the lower pMOS gets out of linear region. When the lower pMOS gets out of linear region,

\[ V_{2} - V_{1} = V_{in} - V_{1} + |V_{ip}|. \]  

The other equations that must be satisfied are

\[ \beta_p((0 - V_{DD} + |V_{ip}|)(V_{1} - V_{DD}) - (V_{1} - V_{DD})^2/2) = \]
\[ \beta_p((V_{in} - V_{1} + |V_{ip}|)(V_{2} - V_{1}) - (V_{2} - V_{1})^2/2) = \]
\[ \beta_p((V_{in} - V_{1} + |V_{ip}|)(V_{2} - V_{1}) - (V_{2} - V_{1})^2/2) = 0.5\beta_n(V_{in} - V_{in})^2. \]  

There are three unknowns \( V_{in}, V_{1}, \text{ and } V_{2} \). There are three equations (1), (2), and (3). Solve them numerically and find the value of \( V_{in} \).

Solving for \( V_{in} \) we get, \( 0 \leq V_{in} < 1.766 \text{ Volts} \).
Consider a four-input priority encoder. It has four inputs \((I_3I_2I_1I_0)\) and three outputs \((O_2O_1O_0)\). Output \(O_2\) is high if and only if all four inputs are low. Outputs \(O_1O_0\) specify the binary encoding of the highest priority high input. Assume \(I_0\) has the highest priority and \(I_2\) has the lowest priority. For example, if \(I_1\) is high and \(I_0\) is low, then irrespective of \(I_3\) and \(I_2\), \(O_1O_0\) must be 01. Use standard cells based design methodology in ICStation to automatically generate a layout for the four-input priority encoder.

Include a printout of logic level schematic and the bounding area of your layout. The layout must pass design rule check (Printout the report to show that it passes design rule check). Do not printout the layout.

**Solution:**

Truth Table

<table>
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<tr>
<th>(I_3)</th>
<th>(I_2)</th>
<th>(I_1)</th>
<th>(I_0)</th>
<th>(O_2)</th>
<th>(O_1)</th>
<th>(O_0)</th>
</tr>
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<td>1</td>
<td>1</td>
<td>1</td>
</tr>
</tbody>
</table>

Therefore from the truth table

\[
O_2 = I_3', I_2', I_1', I_0'
\]

\[
O_1 = I_1', I_0'
\]

\[
O_0 = I_0' (I_2' + I_1)
\]