The exam will be on October 29, 2003, from 7:15 to 9:15 PM in 1240 Computer Sciences. The exam will be closed book except for one 8.5 × 11 sheet of notes.

The other important aspects of the exam are:

1. You should be able to derive the equations that govern the transfer characteristics, noise margins, rise/fall times of any given NMOS or CMOS gate. You need not memorize the equations that we have derived in class or the ones in the text. The gate in the exam will be different from the ones we have derived in class or the ones in the text.

2. You need not memorize design rules, but design rule concepts may be covered.

3. You need not memorize processing steps.

4. You may be asked to informally argue about circuit behavior. For example, what will be the effect of changing the value of $\beta_n/\beta_p$ on the transfer characteristics.

The exam will cover all topics covered in class until the end of the lecture on October 22, 2003. The following is a representative (but not exhaustive) list of topics that will be covered on the exam.

- MOS transistor characteristics including second order effects
- CMOS circuits, transfer characteristics, noise margins, rise and fall times
- CMOS processing concepts
- Design rule concepts
- Clocking strategies: single phase and two phase, Noice’s rules
- CMOS Logic Families: pseudo-nMOS, dynamic gates, domino logic

In terms of the text the exam will cover the following pages: 1–20, 41–58, 61–79, 86–90, 109–123, 142–156, 168–172, 207–226, 295–310, 317–324. Topics discussed in class over and above the material in the text will also be covered in the final. Topics in text which were not covered in class will not be part of the exam.