Spring 2017
Room: KC137
Days: MWF
Time: 12:00-1:50 P.M.

Instructor: Mark Randall
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Course Web Site: *http://csserver.evansville.edu/~mr63/*

Catalog Description: CS 220 Logic Design and Machine Organization (3) Introduction to logic design and computer hardware concepts. Topics include Boolean algebra, number representations, sequential logic, counters and registers, microcomputer architecture and assembly language programming. Prerequisite: None. Spring.

Course Objectives:
Successful students will be able to:

1. Understand the differences between number systems and how to convert between them.
2. To simplify a Boolean expression using Boolean identities and KMAPs.
3. Design a combinational logic circuit.
4. Design a Sequential logic circuit.
5. Construct a digital circuit using digital logic gates.

Texts:

- *Mano, Morris M., and Kime, Charles R., Logic and Computer Design Fundamentals, 5th edition, Prentice-Hall, 2016.*

Software:

- *Logisim*: A digital logic design and simulation program. Logisim is an open source program written in Java, so it runs under all major operating systems. Available for download from ozark.hendrix.edu/~burch/logisim/.
- *Quartus II:* software from www.altera.com. A licensed professional version of this software is available on the CECS server. A student version of this software is available via the internet.

Course Structure: The class will meet three times per week in lecture. Projects and homework will be assigned throughout the semester. Projects and homework will be completed outside of class hours.

Credit Hour Policy: This Course meets the federal requirements of 15 in-class hours plus an expected 30 hours of out-of-class work per credit hour;

Grading:

There will be 4 hour exams, graded homework projects, and a two hour comprehensive final exam. The homework projects will consist of assignments which will be done in teams of three (or less). All exams are open book. The hour exams will count (55/4)% each, the final will count 25%, and the homework projects will count 20% of the final grade. **Class Policies:** Students are expected to abide by the Academic Honor Code. No aid should be given or requested on any examination. Students may collaborate on homework (this is encouraged), but each student must submit their own work. Projects are to be your own work. On programming projects you are not permitted to look at someone else's code nor are you allowed to share your code with someone else.

Office Hours:
MTWTH 10AM-11AM
F 9AM - 11AM

I can be contacted by email anytime between 8:00 AM and 8:00 PM M-F I will respond to email and weekends but only on a limited basis and if I have time and resources to do so.

Disability Policy: It is the policy and practice of the University of Evansville to make reasonable accommodations for students with properly documented disabilities. Students should contact the Office of counseling and Health Education at 488-2663 to seek services or accommodations for disabilities. Written notification to faculty from the Office of Counseling and Health Education is required for academic accommodations.

Honor Code: All students at the University of Evansville agree to the University honor code: I will neither give nor receive unauthorized aid, nor will I tolerate an environment that condones the use of unauthorized aid.

Topics:

1. Binary Numbers and Codes
2. Standard Logic Gates
3. Logic Circuit Simplification
4. TTL and CMOS ICs
5. Encoding and Decoding
6. Arithmetic Circuits
7. Flip Flops and Multi-vibrators
8. Counters and Shift Registers

EE 254 **Spring 2015**

	Monday	Wednesday	Friday
Jan 8	pp. 1-13 Introduction and overview Number systems	pp. 13-31 Arithmetic Ops Alphanumeric codes	pp. 35-54 Boolean algebra Minterms and maxterms
Jan 15	**Martin Luther King Day**	pp. 54-70 Karnaugh maps map manipulation	pp. 65-91 NAND and NOR two-level implementation
Jan 22	pp. 76-91 Integrated circuits High Impedance outputs	Review Ch. 1 & 2	**Ch. 1-2** **Hour Exam 1**
Jan 29		pp. 97-121 Combinational circuits	pp. 122-130 Decoders
Feb 5	pp. 130-148 Decoders and encoders Multiplexors	pp. 149-161 Adders and Subtractors	pp. 161-170 Signed numbers, overflow.
Feb 12	pp. 171-197 VHDL – Verilog Intro	pp. 171-197 Verilog implementation	Review
Feb 19	Ch 3 & 4 **Hour Exam 2**		pp. 207-221 Intro to sequential circuits Flip flops
Feb 26	pp. 221-245 State diagrams sequential design	pp. 240-253 Sequential design JK and D flip flops	pp. 250-280 VHDL and sequential logic
March 5	**Spring Break**	**Spring Break**	**Spring Break**
March 12	pp. 295-310 Design technology Gate delay	pp. 310-330 ROM, PLA, PAL logic devices	pp. 207-330 Review
March 19	Ch. 5-6 **Hour Exam 3**		pp. 335-345 Intro to register transfers
March 26	pp. 345-363 Register transfers Counter design	pp. 350-380 Counter design Microoperations Verilog and counters	**Easter Break**
April 2	pp. 380-402 Verilog counters and registers Intro µprogrammed contr	pp. 413-435 Memory systems SRAM and DRAM	pp. 429-441 SDRAM arrays of DRAM ICs
April 9	pp. 443-471 Review exam	pp. 455-490 Microprogramming Ch 7-8	A simple computer architecture
April 16	Notes and Ch 10 Microprogrammed control	Notes and Ch 10 Review	***NO Class Instructor out of town***
April 23	Course Review		

FINAL EXAM May 2nd @ 11:00 AM